GANPAT UNIVERSITY B.Tech. Semester III (BM), Regular Examination NOV-DEC 2010. BME 302: LINEAR ELECTRONICS

Time: - 3 Hours

A 1

Marks:- 70

- 1. Instructions: Answers to the 2 sections must be written in the separate answer books.
- 2. Figures to the right indicate marks.

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3. Conventional terms or notations are used.

SECTION-I

Q-I	(a)	Justify: The depletion region is wider near the top and narrower near the bottom in JFET	(4)
	(b)	Explain FET as a voltage variable resistance	
	(c)	Describe with neat diagram JFET small signal model	(4)
		OR	(4)
Q.1	(a)	What are the similarities and differences between a BJT and JFET?	(6)
	(b)	Enlist the JFET amplifier configuration and explain common source	(0)
		FET amplifier with neat diagram.	(0)
Q.2	(a)	Draw the neat diagram of n- channel enhancement type MOSFET. And	(6)
		explain its construction, operation and its characteristics in detail.	(-)
	(b)	For the fixed bias circuit, find the values of I_{DQ} , V_{GSQ} and V_{DS} . Assume	(5)
		$I_{DSS}=8mA$ and $V_{p}=-8V$, $R_{D}=2K\Omega$, $R_{G}=1M\Omega$, $V_{DD}=18V$ and $V_{GG}=4V$.	. ,
	(c)	Justify: JFET is a voltage controlled device.	(1)
		OR	
Q.2	(a)	Draw the neat diagram of P- channel JFET and explain its construction	(7)
		operation and its characteristics in detail.	()
	(b)	Compare all FET biasing techniques.	(5)
0.			(-)
Q.3	(a)	Describe with neat diagram the characteristics of silicon controlled	(7)
	(\mathbf{a})	rectifier (SCR) in detail.	• •
	(D)	Explain with neat diagram common gate FET amplifier.	(4)
0-4		SECTION-II	
V ^A	(2)	Explain Transformer coupled Class A small G a total	12)
	(4)	efficiency of Class-A amplifier	
	(b)	Derive equation that shows relationship between emitter to 11	
	(2)	current gain & base to collector current gain for non transistor	
	(c)	In a two port model, $R_{s=1.5KQ}$ Vs=16my Vi=8my $P_{s=0.41KQ}$	
	$\left(\right)$	Av=-170. Find out Vo, Ii, Io, Zi.	
		OR	

Q-4

(12)

- (a) Explain input-output characteristics for Common Emitter configuration.
- (b) What is rectification? Explain in detail Full Wave Rectifier with neat circuit diagram.
- (c) Common base configuration of signal of 10mv is applied across base. Emitter resulting in $I_E=0.5$ mA, if $\alpha=0.98$. determine Zi, Vo, Av, Zo, Ai, I_B
- Q-5
- (a) What is BJT? Draw symbol of npn & pnp transistor. Explain operation of npn transistor.
- (b) What is Darlington connection? Derive equation for AC equivalent & DC bias circuit.
- (c) In dc bias with voltage feedback configuration Vcc=14V, Rc=6.5K Ω , R_B=265K Ω , R_E=1.2K Ω & β = 110 then find out Ic, l_B & V_{CE}.

OR

(12)

(11)

(12)

- (a) Explain the difference between clipper circuits & clamper circuits.
- (b) Calculate β_{dc} & α_{dc} for transistor where Ic is 1.5 mA & I_B is 26µA. Also determine the new base current to give Ic as 5mA.
- (c) Explain effect of negative feedback on gain & bandwidth.

Q-6

(a)

Q-5



Find out VB, Vc, VE, Ic, I_E , and VCE.

- (b) Explain the a.c. analysis of common collector amplifier with neat circuit diagram & Give one application of it.
- (c) Write a short note on Class C amplifier.

END OF PAPER