Seat No.

GANPAT UNIVERSITY

B.TECH. SEM. IV BIOMEDICAL & INSTRUMENTATION ENGINEERING

REGULAR EXAMINATION MAY/JUNE - 2012

2BM403 DIGITAL LOGIC CIRCUITS

TIME -: 3 Hours **TOTAL MARKS -: 70**

Instructions:

1. All the questions are compulsory.
2. Answer of each section must be written in separate answer books.
3. Figure to the right indicate marks.
4. Assume data, if needed.
5. Conventional terms / notations are used.

SECTION-I

Que.1

(a) Implement the Boolean function F = xy + x'y' + y'z [6]

a. With AND, OR and NOT gates
b. With AND and NOT gates
c. With NOR and NOT gates

(b) Convert $(1\,9\,C\,D)_{16}$ to $(\qquad)_{2}$ [6]

Convert $(1\,1\,0\,0\,0\,0\,0\,1\,0\,0\,0\,0\,0\,1\,1)_{BCD}$ to $(\qquad)_{10}$

Convert $(1\,0\,0\,0\,0\,1\,1)_{2}$ to $(\qquad)_{10}$

Que.1

(a) Determine the prime-implicants by tabular method of the function: [7]

$F(w,x,y,z) = \sum(1,4,6,7,8,9,10,15)$

(b) Simplify the following Boolean expressions to a minimum no. of literals: [5]

a. (BC' + A'D) (AB' + CD')
b. xy + y'z + x + xy'z

Que.2

(a) State and prove DeMorgan's theorem for two variables. [5]

(b) Draw and explain J-K flip flop along with truth table diagram. [6]

OR

Que.2

(a) Simplify the Boolean function with K-map and list out the truth table for the simplified function and implement it with logic gates. (any one) [5]

a. $F(w, x, y, z) = \sum(1, 4, 5, 6, 12, 14, 15)$
b. $F(A, B, C, D) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

(b) Explain Half and full adder circuit giving truth table and logic diagram. [6]

Que.3 **Answer any Four:** [12]

(a) Differentiate BCD code and Binary code.
(b) Explain Logical and Universal gates in detail.
(c) Draw and explain T flip flop along with timing diagram.
(d) Convert $(2\,8\,7)_{10}$ to its Octal equivalent. Then convert octal number to binary.
(e) What is the Difference between Digital and Analog Systems?

SECTION-II

Que.4

(a) Implement the Boolean function $F(w,x,y,z) = \sum(0, 2, 3, 5, 10, 14, 15)$ with a multiplexer. [7]

(b) Design a BCD to Excess-3 code converter for decimal digits. Draw its logic diagram. [5]

OR

Que.4

(a) Design a 4 – input priority encoder with input D_0 having the highest priority and D_3 having the lowest priority. [6]

(b) Draw and explain the NOT, NAND and NOR gate implementation using RTL. [6]

Que.5

(a) [6]

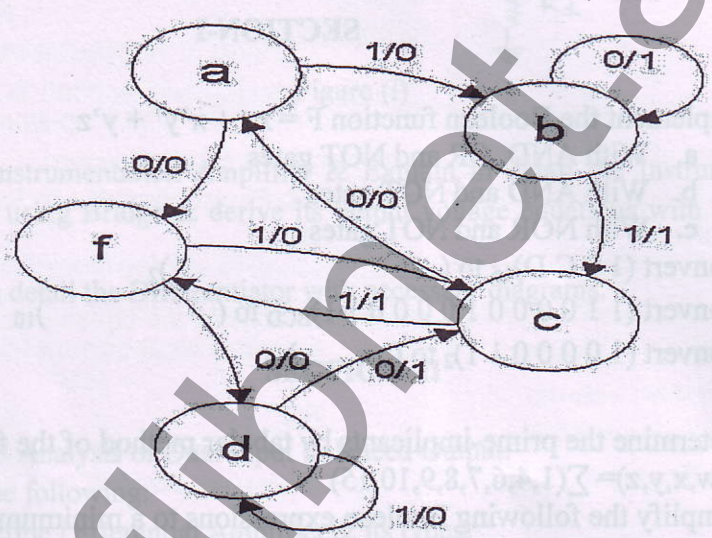

Fig.1

Design state table and state equation for the above state diagram. Use state reduction technique if possible.

(b) Design 3 bit binary counter with logic circuits. [5]

OR

Que.5

(a) Draw and explain the NOT, NAND and NOR gate implementation using DTL. [6]

(b) What is shift register? Draw and explain shift register giving neat diagram. [5]

Que.6 **Answer any Three:** [12]

(a) What are ADC and DAC? Explain the application of ADC and DAC with example.

(b) What is Carry propagation? Explain it with neat diagram.

(c) Draw the block diagram of demultiplexer and explain.

(d) Explain

1). Alphanumeric Code

2). ASCII code

3). EBCDIC code

4). Hollerith code

--END OF PAPER--