Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester: IV (Biomedical & Instrumentation) Engineering

Regular Examination May – June 2014

2BM403 Digital Logic Circuits

Time: 3 Hours **Total Marks: 70**

Instruction: 1Write each section in separate answer book.
2Answer should be brief and to the point.
3 Figure to the right indicates marks.
4Assume suitable data, if necessary.

Section – I

Que. – 1 **12**

a) Define basic logic gates and universal logic gates? Explain the universal gates with logic symbol and truth table.

b) Implement an 8:1 Multiplexer using 4:1 Multiplexer.

OR

Que. – 1 **12**

a) Convert the decimal number 357 in following code:
i) Binary Code ii) Octal Code iii) BCD Code
iv) Gray Code v) Excess -3 Code vi) Hexadecimal Code

b) Draw the logic diagram of 2:4 Demultiplexer using NOR gate only.

Que. – 2 **11**

a) Draw the Half & Full adder Circuit. Make a truth table for it. Also, draw the timing diagram for half adder circuit.

b) Differentiate analog and digital system.

c) Use a Karnaugh map to simply the following SOP expression:
B'C'D' + A'BC'D' + ABC'D' + A'B'CD + AB'CD + A'B'CD' + ABCD'

OR

Que. – 2 **11**

a) Differentiate BCD and Binary number system

b) Using Boolean algebra techniques, simplify following expression:
i) (A' + B) (A + B + D) D'
ii) A C' + B C' D + A B' C + A C D

c) Prove: i) X' (X + Y) + Z' +ZY = Y + Z'
ii) (B + A) (B + D) (A + C) (C + D) = B C + A D

Que. – 3 **12**

a) Answer in short:

i) How many bits are required to represent three digit decimal numbers in BCD?

ii) How many bits are needed to represent decimal values ranging from 0 to 14,556?

iii) When is the output of AND gate is high? What is the IC number of 2 input AND gate?

iv) Convert $(101101)_2$ to gray code.

v) Enlist different non-weighted binary codes.

vi) Which gate is known as inverter?

vii) Find 2's complement of 10110010.

viii) Determine the values of A, B, C and D that make the product term A B' C' D equal to 1.

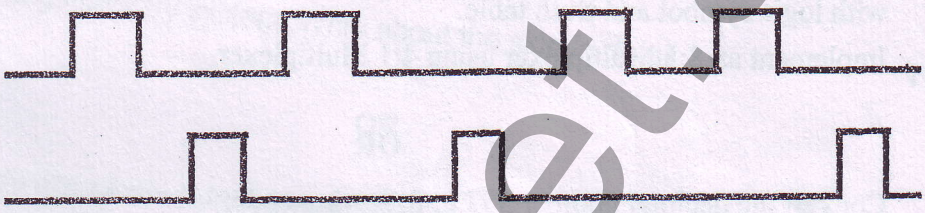
b) Differentiate Combinational and Sequential circuit..

c) Implement with logic gates: A' B + B (A + C') + A B'

Section – II

Que. – 4 12

a) Assume initially Q = 0, Determine Q and Q' waveform for NOR gate latch. Inputs are shown in below figure.



b) Draw the logic symbol, logic diagram of J-K flip-flop and explain in detail.

OR

Que. – 4 12

a) Draw and explain 2 bit asynchronous binary counter with timing diagram.

b) What is the normal resting state of NAND gate as a latch? Explain in detail along with logic diagram and timing diagram.

Que. – 5 11

a) What is the meaning of "SN 74 ALS 08 A" data written on IC? Draw RTL circuit for NOR gate operation and explain its working.

b) Explain R-2R ladder type DAC.

OR

Que. – 5 11

a) Draw and explain the circuit diagram of 1 bit memory cell. Also enlist the assumptions of it.

b) What is the function of shift register? Draw and explain 4 bit serial in – serial out shift register.

Que. – 6 12

a) What is the need of Preset and Clear in S-R flip-flop? Draw the symbol, logic diagram and explain.

b) What is the meaning of "D" in D type flip-flop? What is its application? Draw the logic symbol, logic diagram and explain in detail.

END OF PAPER