Exam No: _____

GANPAT UNIVERSITY

B. TECH SEM- IV (BM&I) REGULAR EXAMINATION– APRIL-JUNE 2016

2BM403 : Digital Logic Circuits

TIME: 3 HRS

TOTAL MARKS: 60

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Que. 01 **Answer the following questions.** [10]

a) Draw the logic symbol and construct the truth table for each of the following gates. [4]
[1] Two input NAND gate [2] Three input AND gate

b) Determine the truth table for the following standard POS expression. [4]
(A+B+C)(A+B'+C)(A+B'+C')(A'+B+C')

c) Using Boolean algebra techniques, simplify following expression: [2]
[AB'(C+BD)+A'B']C

OR

Que. 01 **Answer the following questions.** [10]

a) Do as directed: [5]
1. Convert the decimal number 650 into hexadecimal number.
2. Convert $(1101101101)_2$ to gray code.
3. Convert the binary number 10101.0011 into octal number.
4. Convert $(1\ 9\ C\ D)_{16}$ to ( )$_2$
5. Convert $(1\ 0\ 0\ 0\ 0\ 1\ 1)_2$ to ( )$_{10}$

b) Using Boolean algebra techniques, simplify following expression: [5]
1. (A'+B) (A+B+D)D'
2. AC'+ BC'D + AB'C + ACD

Que. 02 **Answer the following questions.** [10]

a) Minimize the following expressions using Karnaugh map. [8]
1. X(A,B,C,D) = B'C'D' + A'BC'D' + ABC'D' + A'B'CD + AB'CD + A'B'CD' + A'BCD' + ABCD' + AB'CD'
2. F(A,B,C,D) = $\prod$M(1,2,3,8,9,10,11,14)* d(7,15)

b) Define : SSI, MSI, LSI and VLSI [2]

OR

Que. 02 **Answer the following questions.** [10]

a) Obtain the simplified expressions in sum of products for the Boolean function: [6]
F (A,B,C,D,E) =$\sum$(0,1,4,5,16,17,21,25,29)

b) Draw and explain the Layout of three variable Karnaugh map using suitable example. [4]

Que. 03 **Answer the following questions.** [10]

a) Describe the logical functions of the adder, encoder, decoder, multiplexer, de-multiplexer, counter and register. [5]

Que. 03 **b)** Choose the correct answer.

1. The output of a logic gate is 1 when all its inputs are at 0. the gate is either:
   (A) a NAND or an EX-OR (B) an OR or an EX-NOR
   (C) an AND or an EX-OR (D) a NOR or an EX-NOR
2. Determine the values of A, B, C, and D that make the sum term A'+B+C'+D equal to zero.
   (A) A=1,B=0,C=0,D=0 (B) A=1,B=0,C=1,D=0
   (C) A=0,B=1,C=0,D=0 (D) A=1,B=0,C=1,D=1
3. Applying DeMorgan's theorem to the expression $\overline{ABC}$, we get _____.
   (A) $\overline{A} + \overline{B} + \overline{C}$ (B) $\overline{A + B + C}$ (C) $A + \overline{B} + C\overline{C}$ (D) $A(B + C)$
4. The truth table for expression AB+B'C has how many input combinations?
   (A) 1 (B) 2 (C) 4 (D) 8
5. Which of following are known as universal gates
   (A) NAND & NOR. (B) AND & OR. (C) XOR & OR. (D) None.

SECTION: II

Que. 04 **Answer the following questions.** [10]

a) Describe the function of Half-adder and Full-adder with the help of logic symbol, logic diagram and truth table. [6]

b) Draw and explain the working of 3-line-to-8-line decoder with the help of truth table. [4]

OR

Que. 04 **Answer the following questions.** [10]

a) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number. [6]

b) Draw and explain the working of 4-bit parallel adder with the help of suitable example. [4]

Que. 05 **Answer the following questions.** [10]

a) What is the function of shift register? Draw and explain the working of 4 bit serial in-serial out shift register. Assume that the register is initially cleared (all 0s). [5]

b) Explain how the flip-flops can be used for the purpose of frequency division and basic counter applications. [5]

OR

Que. 05 **Answer the following questions.** [10]

a) With necessary sketch explain Bidirectional Shift Register with parallel load. [5]

b) Enlist the types of counter. Explain ring counter with necessary diagrams. Write limitation of it. [5]

Que. 06 **Answer the following questions.** [10]

a) Draw and explain the basic operation of S-R Latch and gated S-R Latch. [5]

b) Draw the state diagram and state table for the circuits shown in Fig.1 [5]

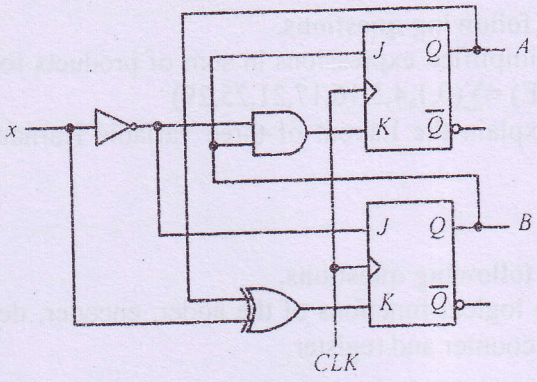

Fig.1

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