Exam No: _____

GANPAT UNIVERSITY

B. TECH SEM- IV (BME) REGULAR EXAMINATION– APRIL-JUNE 2017

2BM403 : Digital Logic Circuits

TOTAL MARKS: 60

TIME: 3 HRS

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Que. 01 **Do as directed:** [10]

1) $(B65F)_{16} = (\_\_\_\_\_)_{10}$
2) $(1010.011)_2 = (\_\_\_\_\_)_8$
3) $(623.77)_8 = (\_\_\_\_\_)_{10}$
4) $(41.6875)_{10} = (\_\_\_\_\_)_2$
5) $(19CD)_{16} = (\_\_\_\_\_)_2$
6) $(4E7.2)_{16} = (\_\_\_\_\_)_8$
7) $(1101110111011110 11)_2 = (\_\_\_\_\_)_{16}$
8) Gray Code representation of $(1110)_2$ is _____.
9) 2's complement of 10110010 is _____.
10) 10110010 ÷ 10 = _____.

OR

Que. 01 **Answer the following questions.** [10]

a) Draw the logic symbol and construct the truth table for each of the following gates. [6]
[1] Four input NAND gate [2] Three input EXOR gate [3] NOT gate

b) Simplify the Boolean functions to a minimum number of literals: [4]
[1] AB'C' + ABC + AB'C + ABC' [2] AB + A'B + A'B'

Que. 02 **Answer the following questions.** [10]

a) Simplify the following Boolean function using K-map [5]
$F(w,x,y,z) = \Sigma(1, 3, 7, 11, 15)$ with don't care condition $d(w,x,y,z)=\Sigma(0, 2, 5)$

b) Explain the Full adder combinational circuit and also design of it with two half adders and an OR gate. [5]

OR

Que. 02 **Answer the following questions.** [10]

a) Given Boolean function: $F= x\,y + x'\,y' + y'\,z$ [5]
1) Implement it with only OR & NOT gates
2) Implement it with only AND & NOT gates

b) Simplify the function $F(w, x, y, z) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$ using K-map with its SOP and POS form. [5]

Que. 03 **Answer the following questions.** [10]

a) Explain the difference between following term with the help of block diagram. [5]
1. Combinational logic circuits & Sequential logic circuits
2. Asynchronous sequential circuits and synchronous sequential circuits

b) Draw the circuit diagram of TTL OR gate, TTL AND gate, TTL NOR gate and TTL NAND gate. [5]

SECTION: II

Que. 04 **Answer the following questions.** **[10]**

a) What is the advantage of using D flip-flop over S-R flip-flop? Explain the working of D flip-flop and S-R flip-flop with the help of logic symbol, logic diagram and truth table. [5]

b) Draw a logic symbol and truth table of the following digital devices. Do not use a gate-level diagram. Label all inputs and outputs. [5]

1. 8-line-to-3-line Encoder with active Low input and Active Low outputs
2. 1-line to 8-line De-Multiplexer

OR

Que. 04 **Answer the following questions.** **[10]**

a) Design a BCD-to-excess-3 code converter with a BCD-to-decimal decoder and four OR gates. [5]

b) Design a combinational circuit that accepts a three bit binary number and generates an output binary number equal to the square of the input number. [5]

Que. 05 **Answer the following questions.** **[10]**

a) Draw and explain Weighted sum and R-2R Ladder D-to-A Converter in detail. [5]

b) Explain the working of 4-bit binary ripple counter with the help of logic diagram and timing waveforms. Assume that the register is initially cleared (all 0s). [5]

OR

Que. 05 **Answer the following questions.** **[10]**

a) Explain BCD Ripple counter and draw its logic diagram and timing diagram. [5]

b) What are the advantages of using universal shift register? Draw and explain the working of 4-bit universal shift register. [5]

Que. 06 **Answer the following questions.** **[10]**

a) What is the function of shift register? Explain the working of 4 bit parallel in-parallel out shift register with the help of logic diagram and the timing waveforms. Assume that the register is initially cleared (all 0s). [5]

b) Explain how the flip-flops can be used for the purpose of frequency division and basic counter applications. [5]

----------END OF PAPER----------