GANPAT UNIVERSITY

B.TECH SEM. VII BIOMEDICAL & INSTRUMENTATION ENGINEERING

CBCS REGULAR EXAMINATION NOVEMBER 2015

2BM503 - MICROPROCESSOR ARCHITECTURE & INTERFACING

TIME: - 3 HOURS TOTAL MARKS: - 70

INSTRUCTION: - 1. Write the answer of each section in separate answer sheet.
2. Figure to the right indicates full marks.
3. Assume suitable data if necessary.

SECTION-I

Que-1 12

(a) Explain Instruction Fetch Operation with suitable figure. 6

(b) Explain Pin diagram of 8085 MPU. 6

OR

Que-1 12

(a) What is timing diagram? Explain timing diagram of byte transfer from memory. 6

(b) Explain Branching Instructions. 6

Que-2 11

(a) Draw and explain architecture of 8085. 6

(b) Explain Peripheral mapped I/O with Suitable figure. 5

OR

Que-2 11

(a) Explain Memory mapped I/O with Suitable figure. 5

(b) Write a Program to sort array of five no's in ascending order from memory. 6

Que-3 12

(a) Define following terms: 4
a) Compiler
b) Interpreter
c) Assembler
d) Operating System

(b) Give difference between Static and Dynamic RAM. 4

(c) Explain latching of low order address bus. 4

SECTION-II

Que-4 12

(a) Draw and explain timing diagram for IN Instruction. 6

(b) Write a program and flow chart for Multiplication of Two no. 6

OR

Que-4 12

(a) Explain Absolute vs. Partial Decoding using suitable figure. 6

(b) Write a program and flow chart to generate a square wave of 200μs time period. Use subroutine. 6

Que-5 11

(a) Write a program and flow chart to convert BCD-To-Hex No. 6

(b) Write a program and flow chart for BCD subtraction with borrow. 5

OR

Que-5 11

(a) Write a program and flow chart to generate square waveform for 5Hz frequency with 50% duty cycle. 5

(b) What is subroutine? Give difference between CALL—RET & PUSH—POP 6

Que-6 12

(a) Identify the address of Input ports given in figure1. 4

(b) Draw and explain generalize programming flowchart. 4

(c) Calculate delay in the following loop, assuming the system clock period is 0.48μs. 4

```
        LXI B,12FF H
Delay:  DCX B
        XTHL
        XTHL
        NOP
        NOP
        MOV A,C
        ORA B
        JNZ: Delay
```

(XTHL-16 T-states, DCX- 6 T-states)

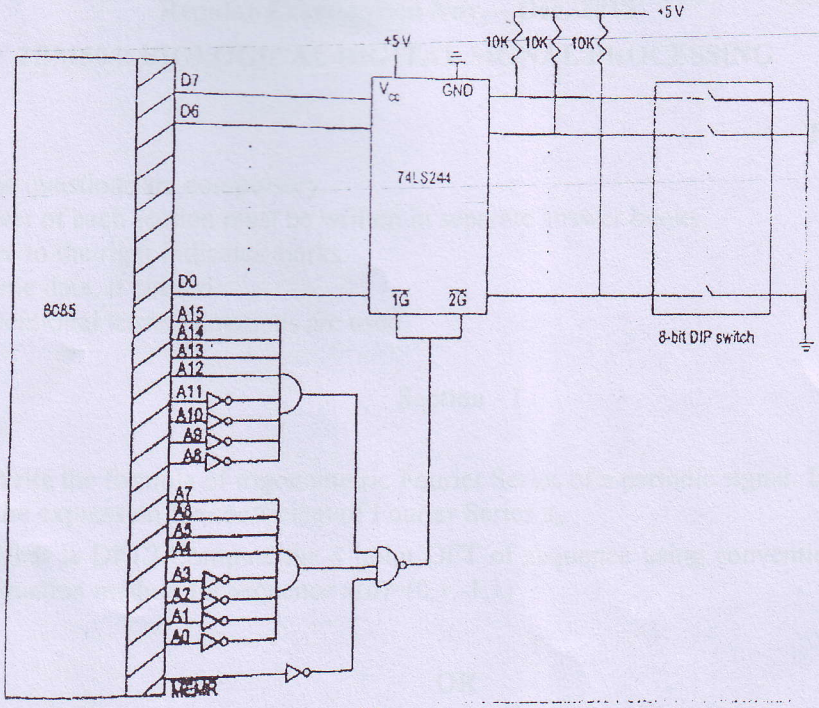

Figure 1

Best of Luck