Exam No._____

# GANPAT UNIVERSITY

**B. Tech Semester – III Computer Engineering**
**Regular Examination November/ December - 2011**
**2CE302: DIGITAL ELECTRONICS**

**Time: 3 Hours]** **[Total Marks: 70**

**Instructions:**

1. Attempt all questions.
2. Figures to the right indicate full marks
3. Each section should be written in a separate answer book

## SECTION-I

1. (A) Answer the following [5]
   (1) Implement NOR gate using basic logic gates.
   (2) Find 10's complement of $(5411.52)_{10}$
   (3) $(1025)_{10}$ = (_____)$_{16}$
   (4) Convert $(1521)_8$ to Hexadecimal.
   (5) Find binary value of $(845)_{10}$
   (B) Prove De' Morgan law [4]
   (C) Express Boolean function F = X +Y'Z in product of sum. [3]

**OR**

1. (A) Answer the following [5]
   (1) Define term: Duality
   (2) Find 9' complement of $(1245)_{10}$
   (3) Implement AND gate using NOR gate
   (4) Find Hexadecimal number of $(1545)_8$
   (5) $(1000111)_2$ = ( _____ )$_{10}$
   (B) List out all postulate and theorem of Boolean algebra. [4]
   (C) Express Boolean function F = X +Y'Z in sum of product [3]

2. (A) Explain Exclusive-OR and Exclusive-NOR gate. [3]
   (B) Minimize the following Boolean function [4]
   F (W, X, Y, Z) = Σ (1, 2, 3, 7, 8, 9, 11, 14, 15) using K-Map Method.
   (C) Implement and discuss full adder using half adder. [4]

**OR**

2. (A) Explain universal gate in brief. [4]
   (B) Minimize the following Boolean function [4]
   F (A,B,C,D) = Σ (0,1, 2, 4 , 8, 10, 14, 15)
   (C) Write a Short note on "Full Subtractor" in brief. [3]

3. Answer the following (Any Three) [12]
   (1) Explain BCD to Excess-3 code conversion in brief
   (2) Simplify the Boolean function F = y' + x'z' and don't care condition d = yz+xy using karnaugh map method
   (3) Draw format for 5 – variable karnaugh map with minterm representation.
   (4) Discuss gray code and parity code in brief.

[P.T.O]

## SECTION-II

4. (A) Answer the following [5]
   (1) What is the difference between register and latch?
   (2) How many of flip- flop are used to design 4- bit register.
   (3) Define term : Carry propagation
   (4) In T-Flip-flop, previous state T= 1 and Q(t) = 1. What will be the value of Q(t+1) when T=1 in current state?
   (5) When race around condition will occur?
   (B) Explain 4- bit binary parallel adder in detail. [4]
   (C) Construct 4 X 16 decoder using 3 X 8 decoder. [3]

**OR**

4. (A) Answer the following [5]
   (1) Define term : Counter
   (2) What will be the value of Q(t+1) if J=K=1?
   (3) What is the important property of combination circuit?
   (4) In D Flip Flop, when D=1 and Q(t) =1, then Q(t+1) =_____
   (5) What is the full form of RTL?
   (B) Write a shot not on "8 X 1 Multiplexer" [4]
   (C) Construct full adder using 3 X 8 decoder [3]

5. (A) Explain Read Only Memory ( ROM ) in detail [3]
   (B) Discuss J-K flip- flop in brief. [4]
   (C) Explain serial transfer in register with an example. [4]

**OR**

5. (A) Explain shift register with an example. [4]
   (B) Discuss Master – Slave J K flip flop [4]
   (C) Explain Programmable Logic Array ( PLA) in detail [3]

6. Answer the following (Any Three) [12]
   (1) Differentiate combinational and sequential circuits.
   (2) Explain serial adder in detail
   (3) Discuss 4- bit register loading with R-S flip flop
   (4) Write a short note on "Octal to Binary Encoder"

**----- END OF PAPER -----**