Exam No._____

GANPAT UNIVERSITY

B. Tech Semester – III (Computer Engineering)
CBCS Regular Examination Nov/Dec 2012
2CE302: DIGITAL ELECTRONICS

Time: 3 Hours] **[Total Marks: 70**

Instructions:

1. Attempt all questions.
2. Figures to the right indicate full marks
3. Each section should be written in a separate answer book

SECTION-I

1. **(A)** Answer the following **[5]**
   (1) Why NAND and NOR gate refer as universal gates?
   (2) $(1F5.63)_{16} = (\_\_\_\_\_)_{10}$
   (3) $(1000111.1)_2 = (\_\_\_\_\_)_8$
   (4) Find 9's complement of $(457815)_{10}$
   (5) Find Complement f=qw+x'y(qr'+rqex')

   (B) Explain basic logic gates in brief. **[4]**

   (C) Write a short note on "Half adder". **[3]**

OR

1. **(A)** Answer the following **[5]**
   (1) How many NAND gates required to built OR gate?
   (2) Find 9' complement of $(512)_{10}$
   (3) $(4561.)_{10} = (\_\_\_\_\_)_{16}$
   (4) Convert 110001111 to gray code
   (5) $(3755)_8 = (\_\_\_\_\_)_2$

   (B) Prove (P+Q)' = P'.Q' and (P.Q)'=P'+Q' **[4]**

   (C) Express Boolean function F = B+A'C in sum of product. **[3]**

2. **(A)** Explain universal gates in details. **[3]**
   (B) Simplify the boolean Function using Tabulation method also find prime implicates. **[5]**
   F(w, x, y, z) = ∑(1,4,6,7,8,9,10,11,15)
   (C) Explain full substractor using half substractor. **[3]**

OR

2. **(A)** Simplify the Boolean Function in SOP and POS form using K'map. **[4]**
   F(A,B,C,D)=∑(0,1,2,4,5,6,9,14) and don't care condition d(A,B,C,D)= ∑ (12,13,8)
   (B) Minimize the following Boolean function **[4]**
   F (A,B,C,D) = Σ (0,1, 2, 4 , 8, 10, 14, 15) using tabulation method.
   (C) List out all postulates and theorem of boolean algebra. **[3]**

3. Answer the following **[12]**
   (1) Explain BCD to Excess-3 code conversion in brief.
   (2) Find substraction 1's Complement 1011110000101010 1-101011110001110101
   (3) Explain 5- variable karnaugh map with an example.

[P.T.O]

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SECTION-II

4. **(A)** Answer the following [5]
   (1) Define term: Register
   (2) How many selection lines are used in 16 X 1 MUX?
   (3) In D Flip Flop, when D=1 and Q(t) =1, then Q(t+1) =_____
   (4) When Race condition will occurs in R-S flip flop.
   (5) Define term : Carry propagation
   (B) Explain 3 X 8 decoder in brief [3]
   (C) Write a short note on BCD Adder [4]

OR

4. **(A)** Answer the following [5]
   (1) Define term : Flipflop
   (2) How many selection lines are used in 32 X 1 MUX?
   (3) What is the important property of combination circuit?
   (4) Define term : Asynchronous Flip flop
   (5) What is the full form of T flip flop?
   (B) Discuss 8 X 3 encoder in details. [4]
   (C) Explain 1 X 8 demultiplexer in brief [3]

5. **(A)** Explain J-K flip flop in brief. [4]
   (B) Explain register with parallel loading using R-S flip-flop [4]
   (C) Write a short note on "Serial adder" [3]

OR

5. **(A)** Explain Bi-directional shift register with parallel load. [4]
   (B) Discuss Master – Slave flip flop [4]
   (C) Explain Programmable Logic Array (PLA) in detail. [3]

6. Answer the following (Any Three) [12]
   (1) Explain T flip flop in details
   (2) Discuss serial transfer in brief.
   (3) Differentiate combinational and sequential circuits.
   (4) Explain EX-OR and EX-NOR gate and also implement using NAND gate

----- END OF PAPER -----

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