[P.T.O]

GANPAT UNIVERSITY

B. Tech Semester – III Computer Engineering Regular Examination November – December 2013 2CE302: Digital Electronics

	Time: 3 Hours] [Tot						
	Instr	 Attempt all questions. Figures to the right indicate full marks. Each section should be written in a separate answer book. 					
SECTION-I							
1.	(A)	Do as directed (1) Perform 1001001 – 101101 using 1's complement method. (2) $(25A.25)_{16} = (___)_{10}$ (3) Convert 1001111 to cyclic code	[5]				
		(4) Find octal value of $(4567)_{10}$ (5) Find 2's complement of 10110111					
	(B) (C)	Implement basic logic gates using NAND and NOR gate Explain error detection code with an example.	[4] [3]				
		OR					
1.	(A)	Do as directed (1) $(A12.21)_{16} = (_\)_8$ (2) Perform 110101 – 1011 using 2's complement method. (3) Define : Duality (4) Find Hexadecimal number of (1020) ₁₀	[5]				
		(5) $(1000111)_2 = ($)10					
	(B) (C)	Implement Exclusive-OR using universal gates Express Boolean function $F = P + Q'R$ in form of Maxterm	[4] [3]				
2.	(A) (B)	Prove $(A+BC'+C)C' = ABC' + AB'C' + A'BC'$ using Boolean algebra Minimize the following Boolean function	[3] [4]				
	(C)	$P(W, X, Y, Z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) using Karnaugh Map method.$ Draw format for 5 variable karnaugh map with minterm representation.	[4]				
2.	(A) (B)	Explain full adder combination circuit with help of Half Adder Minimize the following Boolean function $F(A,B,C,D) = \Sigma(0,1, 2, 4, 8, 10, 14, 15)$ and don't care condition	[4] [4]				
	(C)	$d(A,B,C,D) = \Sigma$ (3,5,8) using K – Map method Implement F= A'B'C + AB + AD' using only basic logic gates.	[3]				
3.	(A)	Answer the following (Any Two) Discuss Tabulation method for simplification of Boolean function with suitable	[12]				
-	(R)	example Implement and Discuss a combinational circuit that convert BCD number to					
		Excess- 3 code					
	(0)	Discuss 4- on magnitude comparator in orier.					

SECTION-II

		and the manual second of the second s		
4.	(A)	Answer the following		[5
		(1) What is difference between ROM and RAM.		
		(2) Define term : Latch	nat a	
		(3) What is the difference between synchronous and asynchronous counter?		
		(4) In JK-Filp-liop, J-1, K-1 and previous output $Q(t) = 1$ then what will be value of $Q(t+1)^2$	e the	
		(5) What is the full name of VI SI?		
	(B)	Explain BCD adder in details.		[4]
	(C)	Implement boolean function $F(A,B,C) = \Sigma (0.2.4.7)$ using multiplexer.		[3]
			•	
		OR		
4.	(A)	Answer the following		[5]
		(1) Define term : Word time		
		(2) What is the difference between register and latch?		
		(3) Define term : Flip Flop		
		(4) In D Flip Flop, when $D=0$ and $Q(t) = 1$, then $Q(t+1) =$		
	(D)	(5) What is the full form of PROM?		141
	(D)	Construct 4 X 16 decoder using 3 X 8 decoder		[4]
	(C)	Construct 4 X to decoder using 5 X 8 decoder		[9]
		a stage to be definition of increases and the second states at some		
5.	(A)	Explain Toggle flip-flop in details.		[3]
	(B)	Write a short note on "Serial Adder"		[4]
	(C)	Write the difference between combinational and sequential circuit.		[4]
		(4) Find Recedeminal authors of ADDA ALL 20, 26018342008		
		OR		
5	(1)	Write a short note on "Sarial Transfor"		[2]
3.	(A) (B)	Discuss Master - Slave I K flip flop in brief		
	(C)	Explain Programmable Logic Array (PLA) in detail.		[4]
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6.		Answer the following (Any Two)		[12
		(1) Discuss 4- bit binary parallel adder with carry propagation mechanism.		
		(2) Explain Bi-directional shift register with parallel load		
		(3) Discuss asynchronous binary ripple counter in brief.		

----- END OF PAPER -----