GANPAT UNIVERSITY

B. Tech. Semester: III (Computer Engineering)

Regular Examination November – December 2014

2CE302: Digital Electronics

Time: 3 Hours

Total Marks: [70]

Instruction:

1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Answer both sections in separate answer sheets.

Section – I

Que.1 (A)	Answer the followings.	[5]
(1)	$(101001011)_2 = (\underline{\hspace{2cm}})_{10}$	
(2)	Convert the decimal number 250.5 into base-3.	
(3)	Find the 9's complement of decimal number $(1457)_{10}$	
(4)	Convert decimal number $(8620)_{10}$ into excess-3 code.	
(5)	Perform Subtraction using 1's complement: $(11001)_2 - (10101)_2$	
(B)	State & prove the associative and distributive law.	[4]
(C)	Express the Boolean function F=x+yz as a sum of minterm form	[3]

OR

Que.1 (A)	Answer the followings.	[5]
(1)	$(630.4)_8 = (\underline{\hspace{2cm}})_{10}$	
(2)	Convert $(1111)_2$ into gray code.	
(3)	$(0.6875)_{10} = (\underline{\hspace{2cm}})_2$	
(4)	$(FFF)_{16} = (\underline{\hspace{2cm}})_{10}$	
(5)	$(673.12)_8 = (\underline{\hspace{2cm}})_2$	
(B)	Express the boolean function F=y'+x'z' in a sum of minterm form and Product of maxterm form.	[4]
(C)	Simplify the boolean function F=P+Q+R+R'+R using postulates.	[3]

Que.2 (A)	Minimize the boolean function in product of sum form $F(A,B,C,D)=\sum (0,2,4,5,7,8,10,12,13,15)$ using Karnaugh map method	[3]
(B)	Minimize the boolean function in sum of product form using K-map $F(P,Q,R,S)=\sum (1,3,7,11,15)$ with don't care condition $F(P,Q,R,S)=\sum (0,2,5)$	[4]
(C)	Explain Full adder combinational circuit.	[4]

OR

Que.2 (A)	Minimize the boolean function in sum of product using K-map F=A'B'C'+B'C'D'+A'BCD'+AB'C'	[3]
(B)	Write short note on "octal to binary encoder".	[4]
(C)	Explain Full subtractor combinational circuit.	[4]
Que.3	Answer the followings.	
(A)	Simplify the boolean function using tabulation method $F(w,x,y,z)=\sum (0,1,2,8,10,11,14,15)$	[5]
(B)	Explain parity generator and parity checker circuit.	[5]
(C)	Difference between combinational and sequential circuit	[2]

Que.4 (A)   **Answer the followings.**   [5]
- (1) What is the full foam of MSI and LSI?
- (2) Define term carry propagation.
- (3) In D flip-flop when D=0 and Q(t)=1 then Q(t+1)=_____
- (4) How many selection lines are used in 32×1 multiplexer?
- (5) In decoder input lines are 3 then how many output lines produce?

(B)   Implement the following Boolean function with a Multiplexer.   [4]
$F(A,B,C,D)= \sum (0,1,3,4,8,9,15)$

(C)   Explain 1×8 Demultiplexer in Details.   [3]

OR

Que.4 (A)   **Answer the followings.**   [5]
- (1) Define term flip-flop.
- (2) When race conditions occur in R-S flip-flop?
- (3) What is difference between latch and register?
- (4) Define term trigger in the context of flip flop.
- (5) What is the full foam of EPROM?

(B)   Explain programmable Logic Array (PLA) in Details.   [4]
(C)   Discuss Master-Slave J-K Flip-Flop.   [3]

Que.5 (A)   Explain Serial adder in Register with block diagram.   [6]
(B)   Draw and Explain the block diagram of 4-bit full-adder with look-ahead carry.   [5]

OR

Que.5 (A)   Draw and explain 4-bit magnitude comparator circuit.   [6]
(B)   Write Short note on "Octal to Binary encoder".   [5]

Que.6 (A)   Write short note on 8×1 multiplexer.   [6]
(B)   Discuss 4-bit Register with parallel loading using R-S Flip-Flop.   [6]

END OF PAPER