Exam No: _____

GANPAT UNIVERSITY

B. TECH SEMESTER - III (COMPUTER ENGINEERING)

REGULAR EXAMINATION NOV- DEC 2016

2CE302: Digital Electronics

TIME: 3 HRS **TOTAL MARKS: 60**

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Que-1 **(A) Answer the following** **[6]**

1. $(1101.1101)_2=(\_\_\_\_\_)_{10}$
2. $(109.125)_{10}=(\_\_\_\_\_)_2$
3. $(1265.731)_8=(\_\_\_\_\_)_{10}$
4. Perform the addition of given number in BCD: (191 + 171)
5. $(E23.351)_{16}=(\_\_\_\_\_)_{10}$
6. What is an excess-3 code of given decimal number: (56).

(B) Prove De Morgan's laws using proper logic diagram and truth table. **[4]**

OR

Que-1 **(A) Answer the following** **[6]**

1. $(766.421)_8=(\_\_\_\_\_)_2$
2. Perform subtraction of given decimal number using 9's complement: (20 – 1000)
3. $(101011011001.1010111)_2=(\_\_\_\_\_)_{16}$
4. Find the sign-magnitude representation of given number using 8 bits: (-123).
5. Find the gray codes for the given binary number: (01011110)
6. What is full foam of EBCDIC?

(B) Simplify the following Boolean functions using K-map method in SOP. **[2]**
$Y(P,Q,R,S)=\Sigma(0,1,2,4,5,8,9,12,13,14)$.

(C) Simplify the Boolean function $F(A,B,C,D)=\Sigma(0,1,2,4,5,8,13)$ together with the don't care condition $d((A,B,C,D)=\Sigma(3,6,7,9,12)$ in SOP and POS. **[2]**

Que-2 **(A)** Design EX-OR and EX-NOR using NAND and NOR gate only. **[3]**

(B) Simplify the given boolean functions using Quine-McCluskey method. **[5]**
$Y=\Sigma(0,2,3,6,7,8,10,12,13)$

(C) Explain combinational circuit that performs addition operations on 2-bit. **[2]**

OR

Que-2 **(A)** Implement and discuss full subtractor using 3×8 line decoder. **[4]**

(B) What is carry propagation delay? Explain any one technique to reduce carry propagation delay time in parallel adder. **[4]**

(C) Implement the given Boolean expression using multiplexer. **[2]**
$Y=(A+B)\cdot (A' + B +C) \cdot (A + B')$

[P. T. O]

Que-3	(A)	Implement the even parity generator combinational logic circuit.	[4]
	(B)	Explain 8×1 multiplexer in details.	[3]
	(C)	Differentiate combinational and sequential logic circuit.	[3]

SECTION: II

Que-4	(A)	**Answer the following**	[5]
	1.	What is importance of don't care condition in karnaugh map method?	
	2.	In D Flip Flop, when D=1 and Q(t)=1 then what is the value of Q(t+1)?	
	3.	Differentiate volatile and nonvolatile memory.	
	4.	How many entries in truth table if magnitude comparator circuit that perform comparison of two 4-bit numbers?	
	5.	How many output lines in an encoder if input lines are 16 .	
	(B)	Implement and discuss the circuit that converts BCD to excess-3 code.	[5]

OR

Que-4	(A)	**Answer the following**	[5]
	1.	In toggle flip-flop the previous input T=1 then output Q(t)=1, so hat is output in next state if T=1?	
	2.	When race condition will occurs in RS flip-flop?	
	3.	What is full foam of EEPROM?	
	4.	What is the importance parity generator and checker combinational circuit?	
	5.	Difference between register and flip flop.	
	(B)	Discuss combinational circuit that converts 4-bit binary number to equivalent gray number.	[5]
Que-5	(A)	Design and explain octal to binary encoder.	[4]
	(B)	Discuss 4-bit binary ripple counter using JK flip flop.	[4]
	(C)	If content of 4-bit shift right register R1=0101 and R2=1101. what is the content of Register R1 and R2 after 3 clock pulse(direction R1→R2)	[2]

OR

Que-5	(A)	Discuss Data latch flip-flop in brief.	[4]
	(B)	Discuss J-K flip-flop in brief.	[4]
	(C)	Draw the circuit diagram of 4-bit up-down binary counter.	[2]
Que-6	(A)	Discuss serial adder in brief.	[5]
	(B)	Explain 4-bit bidirectional shift register with parallel load in details.	[5]

----------END OF PAPER----------