Exam No: _____

GANPAT UNIVERSITY
B. TECH. SEMESTER – V COMPUTER ENGINEERING
REGULAR EXAMINATION NOV / DEC - 2012
2CE503: COMPUTER ARCHITECTURE

TIME:-3 HOURS] **[TOTAL MARKS: 70**

Instructions:

1. Figures to the right indicate full marks.
2. Each section should be written in a separate answer book.
3. Be precise and to the point in your answer.

SECTION – I

Q – 1	(A)	Discuss the phases of Instruction Cycle with flowchart.	4
	(B)	Explain Direct and Indirect Addressing	2
	(C)	Differentiate SIMD and MIMD.	2
	(D)	Explain the following terms	4
		I. Delayed load	
		II. Pipeline conflict	
		OR	
Q – 1	(A)	Explain the following terms.	2
		I. Instruction code	
		II. Operation code	
	(B)	Explain hardwired control organization and microprogrammed control organization.	4
	(C)	Explain different addressing modes with an example.	6
Q – 2	(A)	Write difference between subroutine and interrupt.	6
	(B)	Explain Delayed branch with an example	5
		OR	
Q – 2	(A)	Explain Flynn's classification	5
	(B)	What is array processor? Explain SIMD array processor	6
Q – 3	(A)	List all the three address, two address, one address, zero address and RISC instructions with its examples.	7
	(B)	Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.	5

SECTION – II

Q – 4	(A)	Explain isolated versus memory mapped I/O	6
	(B)	Write the major differences exist between the central computer and I/O peripherals.	6

OR

Q – 4	(A)	Write a short note on modes of transfer.	6
	(B)	Explain Parallel priority Interrupt.	6
Q – 5	(A)	Write a note on CPU-IOP communication.	6
	(B)	Explain match logic in associative memory.	5

OR

Q – 5	(A)	Explain Stack and evaluate the following expression using stack (3+4)*[10(2+6)+8].	6
	(B)	Explain crossbar switch organization.	5
Q – 6	(A)	Explain different dynamic arbitration algorithms	6
	(B)	Explain the following terms.	6

I. Data dependency
II. Hardware interlocks
III. Operand forwarding

END OF PAPER