Student Exam No: _____

GANPAT UNIVERSITY
B. Tech. Semester - V (Computer Engineering)
Regular Examination Dec - 2013
2CE503: Computer Architecture

Time: 3 Hours] **[Total Marks: 70**

Instructions:

1. Figures to the right indicate full marks.
2. Attempt each section in a separate answer book.
3. Be precise and to the point in your answer.

SECTION-I

Que-1 **[A]** What is Register Transfer Language? Discuss Memory Transfer Operation with appropriate symbolic notations. **[6]**

[B] Draw & Explain schematic diagram of 4 bit binary adder – subtractor combinational circuit with truth table. **[5]**

[C] Draw one stage of hardware implementation of circuit that generate four basic (AND, OR, XOR, COMPLEMENT) logic micro operations. **[1]**

OR

Que-1 **[A]** Draw & Explain Micro Programmed Control Organization. **[6]**

[B] Discuss how mapping of instruction code to microinstruction address is carried out in micro programmed control unit. **[5]**

[C] Draw a one stage of Arithmetic Logic Shift unit. **[1]**

Que-2 **[A]** Explain following types of CPU organization **[6]**
1) General Register Organization 2) Stack Organization.

[B] Explain Overlapped Register Windows scheme. **[5]**

OR

Que-2 **[A]** Discuss Destination initiated data transfer using handshaking. **[6]**

[B] Explain Stack organization as a part of Random Access Memory with Push & Pop operation with respect to the content of stack pointer register. **[5]**

Que-3 **[A]** Explain following types of interrupt **[6]**
1) Internal Interrupts.
2) External interrupts.
3) Software interrupts.

[B] Explain Isolated I/O and Memory Mapped I/O Configuration. **[4]**

[C] List RISC Architectures characteristics. **[2]**

SECTION-II

Que-4	[A]	Explain indirect addressing with LDA (Load Accumulator) instruction.	[6]
	[B]	Explain format of following basic computer instruction type 1) Memory Reference instructions. 2) Register Reference instructions. 3) I/O instructions.	[6]
		OR	
Que-4	[A]	Draw a complete flow chart for instruction cycle with timing signals.	[6]
	[B]	Explain the execution of BSA (Branch and save return address) instruction in detail.	[6]
Que-5	[A]	List & Explain Flynn's classifications.	[6]
	[B]	Explain Memory Interleaving.	[5]
		OR	
Que-5	[A]	A system has 6 RAM chips and single Rom chip. Size of each RAM chip is 256 X 16 & size of ROM chip is 1024 X 16.CPU generate 20 bit address Draw a Memory connection scenario.	[6]
	[B]	Explain Arithmetic Pipeline.	[5]
Que-6	[A]	Discuss following Cache Organization with example 1) Associative Mapping 2) Direct Mapping.	[8]
	[B]	Explain Fixed Length Paging scheme for Virtual Memory.	[4]

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