Student Exam No: _____

GANPAT UNIVERSITY
B. Tech. Semester - V (Computer Engineering)
Regular Examination Nov/Dec - 2014
2CE503: Computer Architecture

Time: 3 Hours] **[Total Marks: 70**

Instructions:

1. Figures to the right indicate full marks.
2. Attempt each section in a separate answer book.
3. Be precise and to the point in your answer.

SECTION-I

Q -1 [A] Discuss following micro operations in brief. [8]
1) Arithmetic micro operation. 2) Shift micro operation. 3) Logic micro operation. 4) Data transfer micro operation.

[B] Draw and extend the 3 – bit binary adder circuit that will work as binary incrementer. [4]

OR

Q -1 [A] Draw schematic of Bus system (Bus transfer) for following scenario using Multiplexers. [8]
1) No of registers are four. 2) Size of each register is 4 bit long. 3) Size of data path is four bits.

[B] Explain divides by 2 and multiplies by 2 shift micro operations with example. [4]

Q -2 [A] Discuss the execution of LDA and STA memory reference instructions with appropriate timing signals. Consider addressing mode is direct addressing mode. [6]

[B] Discuss following general purpose registers in brief. [5]
1) PC. 2) AC. 3) IR. 4) MAR. 5) DR.

OR

Q -2 [A] Consider in basic Computer, Following micro operation is performed during time signal X. Write in detail about the control signals generated by the control unit and micro operation performed for each control signal in order to complete the given task. [6]

X: M[MAR] ← PC ,PC ← PC +1

NOTE:

1. All general purpose registers, ALU and Memory unit are connected using common bus structure.
2. PC is 16 bit Register with Three control signal LD, INC, CLR. Binary 101 is given as an input to bus select logic to select PC register.
3. Size of Memory is 512 bytes and has two control signals RD, WR.

[B] Discuss handling of Subroutines call using BSA and BUN instructions in basic Computer Architecture. [5]

Q -3 [A] What is assembly language? Discuss the basic parts of an assembly language program. [6]

[B] Discuss with example how Memory reference instruction is encode (in binary) with direct addressing. Size of memory is 1024 bytes. Given architecture support 14 memory reference instructions. [6]

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SECTION-II

Q-4 [A] Discuss the execution of following instruction in single accumulator based CPU organization. [6]

AND M where M is a specific Memory Location

[B] Explain following addressing modes [6]

1) Base register addressing mode. 2) Program counter based relative addressing mode

OR

Q-4 [A] List the micro operations to perform data transfer operations between accumulator register and stack during program execution when stack is implemented as part of main memory. [6]

[B] Discuss 8086 Architecture as a general purpose register based CPU organization with example. [6]

Q-5 [A] Discuss following architectures [6]

1) SIMD. 2) MIMD.

[B] Discuss with example how CPU interacting with various storage elements (devices) in defined computer architecture. [5]

OR

Q-5 [A] Discuss pipeline processing. [6]

[B] Draw Space- Time Cross Matrix showing the execution of 8 different tasks in pipelined architecture where number of segments in pipelined are 5. [5]

Q-6 [A] Differentiate Static RAM & Dynamic RAM. [6]

[B] Discuss 3 ways Set- Associative Mapping between Main Memory and Cache Memory. [6]

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