Morning
Date: 27/11/2015

Student Exam No. _____

GANPAT UNIVERSITY

B. Tech. Semester: V (Computer Engineering)

Regular Examination November – December: 2015

2CE503: Computer Architecture

Time: 3 Hours | Total Marks: 70

Instructions: 1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Answer both sections in separate answer sheets.

Section – I

Que. 1 (a) Explain hardware implementation for register transfer with diagram and timing signals. 6

(b) Explain hardware implementation diagram of 4-bits combine binary adder-subtractor circuit. 6

OR

Que. 1 (a) Describe construction of a common bus system for three state buffers with diagram. 6

(b) Draw and explain diagram of one stage of an arithmetic-logic-shift unit. 6

Que. 2 (a) Draw and explain block diagram to show basic computer registers connected to a common bus. 6

(b) Explain different types of 16 bits instruction formats for basic computer using figure. 5

OR

Que. 2 (a) Which are the different phases of instruction cycle? Describe register transfer for fetch phase with its diagram. 6

(b) What is the role of sequence counter (SC) in control unit? Explain with the help of its three inputs. 5

Que. 3 (a) Describe second pass of assembler required during translation process with flowchart. 6

(b) Explain following terms: 6

(1) ORG instruction (2) END instruction
(3) DEC instruction (4) HEX instruction
(5) Compiler (6) Program loop

Section - II

Que. 4	(a)	Differentiate hardwired and microprogrammed control unit. Then draw and explain block diagram of control unit of basic computer.	6
	(b)	Draw and explain block diagram of a control memory and the associated hardware needed for selecting the next micro instruction address.	6

OR

Que. 4	(a)	Draw 20 bits microinstruction code format then explain only condition for branching(CD) and branch field(BR) as a part of this format.	6
	(b)	Draw and explain diagram for decoding of microoperation fields with three 3 x 8 decoders.	6
Que. 5	(a)	Define: addressing mode and describe any three addressing modes.	6
	(b)	Compare CISC vs RISC with atleast seven differences between them.	5

OR

Que. 5	(a)	Describe concept of virtual memory with diagram.	6
	(b)	Define: Pipelining, Assume process time of each segment is tp=20ns, pipeline has k=4 segments and executes total n=100 such tasks in sequence, then calculate speedup of pipelining.	5
Que. 6	(a)	Explain direct addressing mapping technique for cache memory.	6
	(b)	Explain use of associative memory in cache memory with diagram.	6

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