Exam No:_____

GANPAT UNIVERSITY

B.Tech. Semester VII (CE/IT)

Regular Examination Nov/Dec-2012

IT704 / CE704: Parallel Processing & Architecture

Time: 3 Hours] **[Total Marks: 70**

Instructions: 1. All questions are compulsory.
2. Answer both sections in separate answer sheets.

SECTION-I

Que.1 **(a)** An examination paper has 4 questions and total number of answer books are 1000. each question takes 5 minutes to correct. If 4 teachers are employed for correction in pipeline mode. Then calculate the speedup and efficiency. **[4]**

(b) Explain four protocols used to handle the problem of concurrent write operation **[4]**

(c) Describe delay due to resource constraints in a pipeline. **[4]**

OR

Que.1 **(a)** Explain configuration of SIMD Array processor with figure. **[4]**

(b) Describe branch prediction buffer. **[4]**

(c) Explain data buffering and busing structures as a principle of designing pipeline processors. **[4]**

Que.2 **(a)** Give any three differences between temporal and data parallelism. **[3]**

(b) Find out delay in number of clock cycle, due to data dependency for the following instructions. **[3]**

Instr. 1. MUL R1,R2,R3
Instr. 2. ADD R3,R4,R5
Instr. 3. INC R2
Instr. 4. SUB R5,R6,R7

(c) Apply internal forwarding technique for the following operations in a sequence. Draw data flow graph and make compound function after applying this method. **[5]**

1. $R_0 \leftarrow (M_1)$ (fetch)
2. $R_0 \leftarrow (R_0) + (M_2)$ (add)
3. $R_0 \leftarrow (R_0) * (M_3)$ (multiply)
4. $M_4 \leftarrow (R_0)$ (store)

OR

Que.2 **(a)** Specify a software method to reduce delay due to branches. **[3]**

(b) Explain Store Register step of instruction execution with block diagram. **[4]**

(c) Describe Masking and Data routing mechanism with all registers for SIMD array processor. **[4]**

Que.3 **(a)** In a typical program, assume that percentage of unconditional branches be 10% and that of conditional branches be 20% and 60% of conditional branches are taken. if ideal speedup is 4,then calculate the new speedup and percentage of loss in speedup due branch instructions. **[4]**

(b) Describe Flynn's architectural classification scheme of computers based on multiplicity of Instruction-Data stream. **[5]**

(c) Write down the necessary condition for RAW and WAW hazard. **[2]**

(d) Define: Precise exception **[1]**

SECTION-II

Que.4 **(a)** Write a parallel program to find factorial of a given number using self scheduling. (Assume number of process=4). **[4]**

(b) Write a parallel program to find average deviation of an integer array of size 300 by using 5 processes by using efficient loop splitting. **[6]**

(c) Describe purpose of barrier. **[2]**

OR

Que.4 **(a)** Write a program to sum all the elements of integer array of size 280. Use total of 7 processes. Use following techniques. **[6]**

1) Loop splitting
2) Self scheduling

(b) Consider X as an integer array of size 101. Write a program which will do the following, **[6]**

X[0] = X[1]
X[1] = X[2]
:
:
X[99] = X[100]

Use efficient block scheduling and two processes to solve.

Que.5 **(a)** Write programs to generate histogram for an integer array of size 400. Use 8 processes. Use loop splitting techniques. **[6]**

(b) Write a user defined function process_fork() by using fork(), which will return total N (entered by user) number of processes, such that all processes must have only one child except last process. **[5]**

OR

Que.5 **(a)** Write a program to multiply matrix into vector, Size of matrix is 10*10 and vector is 10. Use indirect scheduling, use total 16 processes. **[5]**

(b) Define speedup and Ideal speedup. **[6]**

Find speedup for the following.

```
for(i=id/t; i<n; i=i+nproc/t)
{
  for(j=id%t; j<n; j=j+t)
  {
//work
}
}
```

nproc = 16, n=10 and t= 6
nproc = 6, n=4 and t= 2

Que.6 **(a)** Write user define function for the followings and explain each. **[6]**

1) To solve contention problem (i.e. init_lock(), spin_lock(), spin_unlock())
2) To solve race condition (i.e. init_barrier(), barrier())

(b) Consider seven integer arrays A, B, C, D, E, F & X. Let their size be 100. Write a program to achieve following. **[6]**

X[0] = A[0] + B[0] + C[0] + D[0] + E[0] + F[0]
X[1] = A[1] + B[1] + C[1] + D[1] + E[1] + F[1]
:
:
X[99] = A[99] + B[99] + C[99] + D[99] + E[99] + F[99]

Use four processes. Use expression splitting with multiple barrier technique.