Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester VII (Computer Engineering/Information Technology)
Regular Examination November – December 2013

2CE703/2IT703: Parallel Processing & Architecture

Time: 3 Hours **Total Marks:** 70

Instruction: 1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Answer both sections in separate answer sheets.

Section – I

Que. 1 **(a)** Write a parallel program to multiply all elements of an array having 9 sizes by using 6 processes. Use following techniques. **10**

I. Loop splitting
II. Self scheduling

(b) Explain what is race condition? **2**

OR

Que. 1 **(a)** Write a parallel program to compute the skewness of a set of data in array having 400 sizes by using loop splitting, use total 8 processes. **6**
[Hint. Skewness = (((a[0]-avg)^3 + (a[1]-avg)^3 + ... + (a[399]-avg)^3) / 400)]

(b) Consider A as an integer array of size 101. Write a parallel program which will do the following, **6**

```
A[0] = A[1]
A[1] = A[2]
  :
  :
A[99] = A[100]
```

Use efficient block scheduling and two processes to solve.

Que. 2 **(a)** Write a user defined function process_fork() by using fork(), which will return total N (entered by user) number of processes, such that all processes must have only one child except last process. **6**

(b) Write a parallel program to count a particular number (entered by user) repeated in the array having 300 sizes by using self scheduling, use total 3 processes. **5**

OR

Que. 2 **(a)** Define speedup and Ideal speedup. Find speedup for the following. **6**

```
for(i=id; i<n; i=i+nproc)
{
        //work (t time);
}
```

1. nproc = 16, n=10,20,30,100
2. nproc = 10, n=10,20,30,100

(b) Write a parallel program to multiply matrix into vector. Size of matrix is 10*10 and array is 10. Use variation on self scheduling with multiple barriers, use total 16 processes. **5**

Que. 3 **(a)** Consider nine integer arrays A, B, C, D, E, F,G,H & X. Let their size be 200. Write a parallel program to achieve following. **6**

```
X[0] = A[0] + B[0] + C[0] + D[0] + E[0] + F[0]+G[0]+H[0]
X[1] = A[1] + B[1] + C[1] + D[1] + E[1] + F[1]+G[1]+H[1]
  :
  :
```

Use four processes. Use expression splitting with multiple spin_lock technique.

(b) Write all possible output for the following programs:

1)
```
main()
{
 int i,fa=1,a,id;
 a=5;
 id=process_fork(5);
for(i=id+1;i<=5;i+=5)
 {
  fa=fa*a*i;
 }
 process_join(id,3);
 printf("%d",fa);
 }
```

2)
```
main()
{ int id,i=5;
printf('Hello\n");
id=fork();
if(id>0)
i=i+50;
wait(0);
printf(%d",i);
}
```

3)
```
main()
{
 int id;
id=fork();
id=fork();
printf("%d",id);
}
```

Section – II

Que. 4 (a) Explain data parallelism with dynamic assignment and derive formula to calculate speedup. **6**

(b) Specify merits and demerits of data parallelism method. **6**

OR

Que. 4 (a) Describe Multiple Instruction Multiple Data stream and Multiple Instruction single Data stream type of computer organization in flynn's classification with figure. **6**

(b) Explain Execution phase of instruction execution with block diagram. **6**

Que. 5 (a) An examination paper has 4 questions and total number of answer books is 900, each question takes 5 minutes to correct. If three pipelines are employed for correction with 4 teachers in each of the pipeline. Then calculate the speedup and efficiency. (distribution time is negligible) **6**

(b) Explain subdivision and replication method to solve a problem of bottleneck in pipeline with figure. **5**

OR

Que. 5 (a) Describe scheme of architectural classification for computers based on serial versus parallel processing. **6**

(b) Specify a software method and register forwarding technique to reduce delay due to control instructions with example. **5**

Que. 6 (a) Describe branch target buffer method to reduce delay due to branch instructions. **6**

(b) If the percentage of unconditional branches is 5%, that of the conditional branches is 15% and immediate instruction is 10%, then find out average number of clock cycles per instruction **3**

(c) A non pipelined computer uses a 10 nsec clock. The average number of clock cycles per instruction required by this machine is 3.85, when the machine is pipelined it requires a 11nsec clock, find out the speedup due to pipelining. **3**

------END OF PAPER------