GANPAT UNIVERSITY

B. Tech. Sem. III (EC) Regular Examination November-December 2011

EC302: Electronic Devices & Circuits

		E C			Total Marks: 70
Ti	me: 3	Hours		AT HAR SHEET HARRY TO MAKE	1 Otal Marks
	structi				ol montal)
		11 4	vanident bas noval	anarate answer hooks.	A DECEMBER OF THE PARTY OF THE
	2 4	newers to the two se	ctions must be written in s	eparate answer social.	Daniel 3 (hit)
	3. F	igures to the right inc	licate full marks.		
	4. A	Assume suitable data,	SECTI	ON-I	5 (A) Draws that
			SEC II	with Doload line.	6
1	(A)	Explain collector ch	aracteristics curve for BJT	rated for figure (a).	6
	(B)	Determine whether	or not the transistor is satu	Tatou isi	
		Assume $V_{CE(sat)} = 0$.	U)	R	LEADING SILL
	(4)	Emploin in detail tra	nsistor as a switch and as a	an amplifier.	6 Morandox (A) 6
1	(A)	Determine In Ic. le	V_{CE} and V_{CB} for figure (t	o). $(\beta_{DC} = 120)$	Last sense (20)
	(B)	Determine 18, 10, 12		a Fig. bies sireuit	and explain O-point 5
2	(A)	Derive equation of	I _B , I _E , I _C , V _B , V _E and V _C	for Emitter bias circuit	and explain &
	()	stability for emitter	bias circuit. common emitter amplifie	r aircuit Draw its AC ed	auivalent circuit and 6
	(C)	Draw and Explain	common emitter amplification, input resistance, outp	ut resistance, current gair	and power gain.
					(C) For a JFE
		D. tamaina V - and	Ic for the pnp transistor c	ircuit of figure (c).	of below figure (d). 4
2	(A)	Determine Ver and	Io for the php transistor c	biased transistor circuit	of below figure (a).
	(B)	(0 - 100)			2
	(C)	What is the main d	isadvantage of base bias n	nethod?	
	(0)	111111111111111111111111111111111111111		in Drow its AC e	quivalent circuit and 4
3	(A)	Draw and Explain	common base amplifier	out resistance current gai	n and power gain.
		Derive its voltage	gain, input resistance, out	par registaries, see	4
	(B)	Explain direct cou	pled two-stage amplifier. ography process and Ion in	nplantation for IC fabric	ation, 4
	(C)	Explain Photolithe	graphy process and for m		$V_{\rm CC}$
				<i>V</i> _{EE} +10 V	+10 V
		Tan Van		Ŷ	
		RC \$1.0kD	$R_{\rm C} \gtrsim 200 \Omega$	n.	R_1 R_C
			$R_{\rm B}$	$R_{2} \geqslant R_{2} $ $10 \text{ k}\Omega \qquad R_{E}$	$ \begin{cases} R_1 \\ 10 \text{ k}\Omega \end{cases} \begin{cases} R_C \\ 1.0 \text{ k}\Omega \end{cases} $
	R	B	AAA — I	VCC	
	-	$\beta_{DC} = 110 = \frac{V_{CC}}{12V}$	7- 24kΩ T-	9V $\beta_{DC} = 150$	
		KO T-12V	V _{BB} + 24 K32		
V	1	With the second	5V T	P Ra	$\begin{array}{c} R_2 \\ \begin{array}{c} \\ \\ \\ \end{array} & \begin{array}{c} \\ \\ \end{array} & \begin{array}{c$
1')				$ \begin{array}{c} R_2 \\ 5.6 \text{ k}\Omega \end{array} $
4	-				
	matrice COSCO-	count to	polatri polatri siti	description descri	Figure (d)
		Figure (a)	Figure (b)	Figure (c)	Figure (a)

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SECTION-II

1	(4)	Give a brief note on reverse recovery time for P-N junction.	4				
*	(A) (B)	Explain the working of schottky diode and photo diode.	4				
	(C)	Explain space charge region, electric field intensity and electrostatic potential for P-N	4				
	()	junction.	•				
		OR CONTRACTOR OF THE PROPERTY					
4	(A)	What is current Density? Derive equation for current density and relate it with	4				
	(B)	Explain diffusion capacitance and transition capacitance.	4				
	(C)	Define:	4				
	(-)	(i) Fermi level					
		(ii) Einstein relationship between diffusion and mobility					
		(iii) Contact potential	4				
5	(A)	Derive the equation of critical frequency(fc) for	5				
	(**)	(i) Low frequency input RC circuit					
		(ii) Low frequency bypass RC circuit, with necessary circuit diagrams					
	(B)	Derive high frequency input RC circuit for BJT amplifier in figure (e). Also determine	6				
		the critical frequency. βac=125, Cbe=20pF, Cbc=2.4pF.					
à	(4)	OR Explain total amplifier frequency response. Also explain unity gain frequency (fT). 5					
5	(A) (B)	Explain total amplifier frequency response. Also explain unity gain frequency (fT). Derive the equation of critical frequency of the bypass RC circuit for the amplifier for					
	(D)	figure (f).					
6	(A)	Why biasing is required? Explain the self-biasing in detail for a n-channel JFET.	4				
	(B)	For a JFET, Explain forward transconductance and voltage divider biasing.	4				
	(C)	For a JFET Vp=6v and maximum drain current is 3mA. The value of forward	4				
		transconductance is 5000 μ S at $V_{OS} = 0$. Find out the value of drain current I_D and					
		forward transconductance at V_{GS} = -4V.					
		$\frac{V_{\text{CC}}}{+10 \text{ V}}$					
		$\begin{array}{c} R_{C} \\ \geq 2.2 \text{ k}\Omega C_{3} \\ \text{Vout} \end{array}$					
	R	$C_1 = \frac{1}{2} \log \Omega$					
	W	R_L R_L R_L R_L R_L					
	600	$\Omega = 10 \mu\text{F}$ $2.2 \text{k}\Omega = 1.0 \text{k}\Omega = 10 \mu\text{F}$					
V _{in} (2	$ \begin{cases} R_2 \\ 4.7 \text{ k}\Omega \end{cases} = \begin{cases} R_E \\ 470 \Omega \end{cases} = \begin{cases} C_2 \\ 10 \mu\text{F} \end{cases} $ $ V_{in} \bigcirc $ $ \begin{cases} R_2 \\ R_2 \end{cases} = \begin{cases} R_E \\ C_2 \end{cases} = \begin{cases} C_2 \\ C_2 \end{cases} = C_2 \\ C_2 \end{cases} = \begin{cases} C_2 \\ C_2 \end{cases} = C_2 \\ C_2 \\ C_2 \\ C_2 \end{cases} = C_2 \\ C_2 \\ C_2 \\ C_2 \end{cases} = C_2 \\ C_2 \\ C_2 \\ C_2 \\ C_2 \end{cases} = C_2 \\ C_$					
	4						
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		Figure (e) Figure (f)					
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