GANPAT UNIVERSITY
B. Tech. Sem. III (EC)
Regular Examination Nov/Dec 2012
2EC304: Digital Electronics

Time: 3 Hours] **[Total Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

1 (A) Write a short note on different digital IC logic families. **6**

(B) Write down the advantages of TTL and CMOS logic families in tabular form. **6**

OR

1 (A) Draw and explain the circuit diagram of DTL basic NAND gate. **4**

(B) Explain with the help of table various versions and characteristics of TTL logic family. **4**

(C) Write a short note on switching time with reference to logic gate. **4**

2 (A) Draw and explain the JK flip flop using NAND implementation. **4**

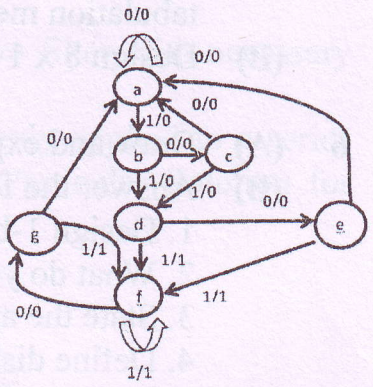
(B) Write a short note on triggering of flip flops. **4**

(C) Draw the excitation tables of all flip flops. **4**

OR

2 (A) Explain the difference between synchronous counter and ripple counter. Design a three bit ring synchronous counter using T flip flop. **6**

(B) Reduce the following state diagram, mention all steps clearly and draw the reduced state diagram. **6**



3 (1) Convert 7654321 to octal. **1**

(2) Convert 5.2545 to binary. **1**

(3) Obtain 10's complement of 21210. **1**

(4) Obtain 2's complement of 100110. **1**

(5) Subtract M=1010101 from N=1001000. **1**

(6) Convert 12345 into BCD. **1**

(7) Convert 1010101 to Gray code.

(8) Convert (11001100)g to Binary code.

(9) Which gate is used in parity generator and checker?

(10) Write our college name in an eight bit code made up of the seven ASCII bits and an even parity bit in the most significant position. Include blanks between names. 2

SECTION-II

4 (A) Reduce the following expressions using identities. 4
(A+C+D)(A+C+D')(A+C'+D)(A+B')

(B) Implement the following. 4
1.Basic gates using NAND gate
2.Basic gates using NOR gate

(C) Find the compliment of following expression 2
(BC'+A'D)(AB'+CD')

(D) Significance of Demorgan's theorem 2

OR

4 (A) Express the following function in sum of minterms and product of maxterms. F(w,x,y,z) = y'z+wxy'+wxz'+w'x'z 4

(B) Simplify using K-map F (A,B,C,D)=$\sum$m(0,2,4,5,6,8,10,15). Draw gate level implementation also Implement the Reduced function using NAND gate only. 8

5 (A) Design Binary Coded Decimal to Excess-3 code conversion using K-Map. 6

(B) Draw and explain a 3 to 8 line decoder. 5

OR

5 (A) Simplify the Boolean function F(A,B,C,D) = $\sum$m(0,1,2,8,10,11,14,15) using tabulation method. 8

(B) Design 8 x 1 Multiplexer using two 4 x 1 Multiplexer 3

6 (A) Draw and explain 4 bit binary parallel sub tractor. 4

(B) Answer the following.
1. Design 1-bit magnitude comparator 2
2. What do you mean by fanin and fanout? 2
3. State the advantages of complex MSI devices over SSI gates 1
4. Define distributive law. 1
5. Find the value of X = A B C (A+D) if A=B=C=D=1 1
6. Define Truth table. 1