GANPAT UNIVERSITY B. Tech. Sem. III (EC) Regular Examination Nov/Dec 2013 2EC304: Digital Electronics

Time: 3 Hours]

Instructions:

- 1. Attempt all questions.
- 2. Answers to the two sections must be written in separate answer books.
- 3. Figures to the right indicate full marks.
- 4. Assume suitable data, if necessary.

SECTION-I

- 1 (A) List and explain different parameters based on which digital integrated circuits are 4 classified.
 - (B) Compare different versions of TTL with reference to the evaluation parameters, in 4 the form of a table.
 - (C) Draw the circuit diagram of three different types of output configuration of TTL 4 gates.

OR

- 1 Design the sequential circuit described by the following state equations. Use JK FF and 12 Mention clearly all the design steps of clocked sequential circuit.
 - A(t+1) = xAB + yA'C + xy
 - B(t+1) = xAC + y'BC'
 - C(t+1) = x'B + yAB'
- 2 (A) Design a counter with following binary sequence: 0, 1, 3, 2, 6, 4, 5, 7 and repeat.
 (B) Design a synchronous BCD counter using T flip flop.

OR

- 2 (A) Draw and explain the block diagram of 4-bit universal shift register.
 - (B) Draw and explain the logic diagram of 4-bit binary ripple counter with the help of 6 its state table.
- 3 Do as directed.
 - (1) Convert 34.5678 to octal.
 - (2) Convert 9123.321 to binary.
 - (3) Obtain 10's complement of 3876809.
 - (4) Obtain 2's complement of 11001100.
 - (5) Subtract M=1010101 from N=1001000.
 - (6) Convert 2358.897 into BCD.
 - (7) Convert 1010101 to Gray code.
 - (8) Convert (11001100)g to Binary code.
 - (9) Convert (110.111101011)₂ in to Octal.
 - (10) Convert (110.111101011)₂ in to Hexadecimal.
 - (11) What is ASCII Code? Explain in brief.

[Total Marks: 70

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SECTION-II

4	Reduc	the following expression to the required number of literals.	
	(A)	ABC + A'B'C + A'BC + ABC' + A'B'C' to five literals.	3
	(B)	BC + AC' + AB + BCD to four literals.	3
	(C)	[(CD)' + A]' + A + CD + AB to three literals.	3
	(D)	(A + C + D) (A + C + D') (A + C' + D) (A + B') to four literals.	3
		OR	
4	(A)	Express the following function in sum of minterms and product of maxterms.	4
		F(w,x,y,z) = y'z + wxy' + wxz' + w'x'z	4
	(B)	Simplify using K-map F (P, Q, R, S) = π M (0, 1, 2, 3, 6, 7, 13, 15). Implement	4
		the reduced function using NOR gate only.	1
	(C)	Demonstrates by means of truth tables the validity of the following theorems of	4
		Boolean algebra.	
		(a) The Associative laws.	
		(b) De Morgan's Theorems for three variables.	
5	(A)	Design the combinational circuit with 3 inputs and 1 output. The output is 1 when	4
2	(A)	the binary value of the inputs is less than 3. The output is 0 otherwise.	
	(B)	Design a combinational circuit that accepts a three bit number and generates an	4
	(2)	output binary number equal to the square of the input number.	
	(C)	Show how a full-adder can be converted to a full-subtractor with the addition of	4
		one inverter circuit.	
		OR	
5	(A)	Simplify the Boolean function using K-MAP, $F(A,B,C,D) = \sum m (2,4,6,8,10) +$	4
		$\sum d(0,1,3)$. Draw the logic diagram from the derived Boolean equation.	4
	(B)	Design 8 x 1 Multiplexer using two 4 x 1 Multiplexer	4
	(C)	Draw five different logic diagrams of various implementations of nan adder.	T
6	Do a	s directed.	1
	(1)	Draw the excitation table of JK hip hop.	1
	(2)	How many EF are required for Modulo 7 counter?	1
	(3)	Write the disadvantage of Asynchronous counter?	1
	(7)	List out the advantages of Master Slave FF compare to normal FF?	1
	(6)	What is the advantage of JK FF over SR?	1
	(0) (7)	Draw the circuit symbol of different triggering mechanism of FF?	1
	(8)	What is the difference between combinational logic circuit and sequential logic	1
		circuit?	
	(9)	What is multiplexer?	1
	. (10)	How many 4-bit binary parallel adders are required for 4- bit BCD adder?	1
	(11)	How can we convert SR FF into D FF?	1
		(in Correct (10) (1) (a) (i) (a) (i) (a) (i) (i) (i) (i) (i) (i) (i) (i) (i) (i	