Morning
Date: 04/12/2014.

GANPAT UNIVERSITY
B. Tech. Sem. III (EC) CBCS
Regular Examination Nov/Dec 2014
2EC304: Digital Electronics

Time: 3 Hours] **[Total Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

1 (A) Write a short note on switching time with reference to logic gate. 4

(B) Draw and explain the circuit diagram of DTL basic NAND gate. 4

(C) Draw the circuit diagram of three different types of output configuration of TTL gates. 4

OR

1 (A) Reduce the following expressions using identities. 4
(A+C+D)(A+C+D')(A+C'+D)(A+B')

(B) Implement the following. 4
1.Basic gates using NAND gate
2.Basic gates using NOR gate

(C) Given the following Boolean function: 4
F = xy'z + x'y'z + w'xy + wx'y + wxy
(a) Draw the logic diagram using the original Boolean expression.
(b) Simplify the function to a minimum number of literals using Boolean algebra.

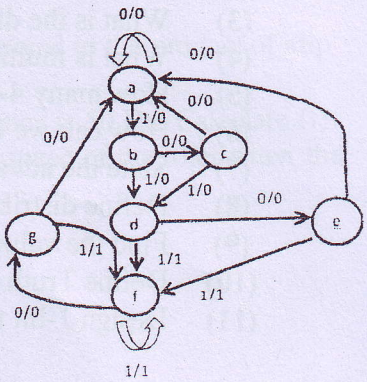
2 (A) Simplify the Boolean function F(A,B,C,D) = ∑m(0,1,2,8,10,11,14,15) using tabulation method. 6

(B) Design a synchronous BCD counter using T flip flop. 6

OR

2 (A) Draw and explain the block diagram of 4-bit universal shift register. 6

(B) Reduce the following state diagram, mention all steps clearly and draw the reduced state diagram. 6



3 **Do as directed.**

(1) Convert 34.5678 to octal. 1

(2) Convert 9123.321 to binary. 1

(3) Obtain 10's complement of 3876809. 1

(4) Obtain 2's complement of 11001100. 1

(5) Subtract M=1010101 from N=1001000. 1

(6) Convert 2358.897 into BCD. 1

(7) Convert 1010101 to Gray code. 1
(8) Convert (11001100)g to Binary code. 1
(9) Convert $(110.111101011)_2$ in to Octal. 1
(10) Convert $(110.111101011)_2$ in to Hexadecimal. 1
(11) What is ASCII Code? Explain in brief. 1

SECTION-II

4 (A) Draw and explain the JK flip flop using NAND implementation. 4
(B) Write a short note on triggering of flip flops. 4
(C) Draw the excitation tables of all flip flops. 4

OR

4 (A) Realize XOR and XNOR gates using (a) Only NAND gates (b) Only NOR gates. 4
(B) Simplify using K-map F (P, Q, R, S) = π M (0, 1, 2, 3, 6, 7, 13, 15). Implement the reduced function using NOR gate only. 4
(C) Demonstrates by means of truth tables the validity of the following theorems of Boolean algebra. 4
(a) The Associative laws.
(b) De Morgan's Theorems for three variables.
(c) The distributive law of + over *.

5 (A) Design a Counter that follows pattern 0,2,3,6,7 and Repeat use JK F/F. 4
(B) Design a combinational circuit that accepts a three bit number and generates an output binary number equal to the square of the input number. 4
(C) Draw and explain a 3 to 8 line decoder. 4

OR

5 (A) Simplify the Boolean function using K-MAP, F(A,B,C,D) = ∑m (2,4,6,8,10) + ∑d (0,1,3). Draw the logic diagram from the derived Boolean equation. 4
(B) Design 8 x 1 Multiplexer using two 4 x 1 Multiplexer 4
(C) Design a Counter that follows pattern 0,2,3,6,7 and Repeat use T F/F. 4

6 **Do as directed.**
(1) How can we convert Ex-OR gate into a NOT gate. Draw the logic symbol. 1
(2) List out the advantages of Master Slave FF compare to normal FF? 1
(3) What is the difference between combinational logic circuit and sequential logic circuit? 1
(4) What is multiplexer? 1
(5) How many 4-bit binary parallel adders are required for 4- bit BCD adder? 1
(6) How can we convert SR FF into D FF? 1
(7) State the advantages of complex MSI devices over SSI gates. 1
(8) Define distributive law. 1
(9) Find the value of X = A B C (A+D) if A=B=C=D=1. 1
(10) Define Truth table. 1
(11) Design 1-bit magnitude comparator. 1