Exam No: _____

GANPAT UNIVERSITY

B. TECH SEM-III (EC)

CBCS(New) REGULAR EXAMINATION– NOV-DEC 2015

2EC302: Digital Electronics

TIME: 3 HRS **TOTAL MARKS: 60**

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.
(4) Assume suitable data, if necessary.

SECTION: I

Que:1 **(A)** List out the basic gates. Draw and explain NAND and NOR equivalent circuits for each. 5

(B) Draw the circuit diagram and truth table for given Boolean expression. Redraw the circuit diagram after simplification. 5
F = x'yz + x'yz' + xz

OR

Que:1 **(A)** Implement Full adder with two half adder and an OR gate. Explain its working. 5

(B) Prove that 1) AB+A(B+C)+B(B+C) = B+AC 4
2) (AB'+AC')(BC+BC')(ABC) = 0

(C) How does the look ahead carry generator speed up the addition process? 1

Que:2 **(A)** What is Multiplexer? Design 8*1 multiplexer using two 4*1 multiplexer and explain its working. 5

(B) Reduce the following expression using k-map and implement it using NAND gate. 5
F= $\sum$m(0,1,4,5,6,7,9,11,15) + d(10,14)

OR

Que:2 **(A)** Design and explain 4 bit binary parallel adder. How to convert it in to binary subtractor? 5

(B) Simplify the function F= Σm(0,1,6,7,8,9,13,14,15) using tabulation method. 5

Que:3 **(A)** Design BCD to excess-3 code converter using 4 bit full adder MSI circuit. 3

(B) State and prove De Morgan's theorem for two variables. 2

(C) Design 2-bit magnitude comparator. 3

(D) Design 2-bit odd parity generator. 2

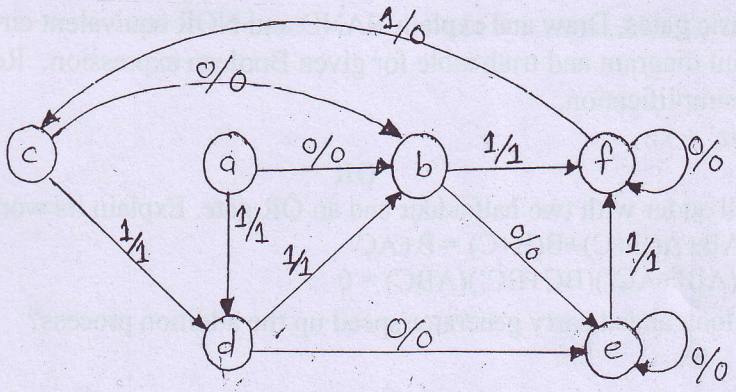
SECTION:II

Que:4	(A)	List out the advantages of CMOS logic family. With the help of neat diagram explain the working of CMOS inverter gate.	5
	(B)	What is register? Construct 4-bit parallel in serial out shift register using D flip-flop. Explain its working.	5

OR

Que:4	(A)	Design and explain 4 bit binary asynchronous counter using appropriate flip-flops.	6
	(B)	List out logic family. Explain them in brief.	4

Que:5	(A)	What is race around condition? How is it eliminated in master slave JK flip-flop?	6
	(B)	Obtain reduced state table and draw the reduced state diagram for the following state diagram.	4



OR

Que:5	(A)	Design 2 bit grey code up counter.	4
	(B)	Explain T flip-flop using NAND gates.	4
	(C)	Differentiate combinational and sequential circuits	2

Que:6	(A)	Convert following number into decimal: (a) $(1234)_5$ (b) $(543)_6$ (c) $(110101)_2$ (d) $(778)_9$	2
	(B)	Convert $(4F7.A8)_{16}$ to binary and octal.	2
	(C)	Perform the operation $(274)_{10}$-$(86)_{10}$ using r's and (r-1)'s complement.	2
	(D)	Find the compliment of F = x'yz'+x'y'z	1
	(E)	Generate 3 bit reflection code.	2
	(F)	Express the Boolean function from SOP to POS F = (x'y + xy')	1

End of Paper