Student Exam No._____

GANPAT UNIVERSITY
B. TECH. SEMESTER III (ELECTRONICS AND COMMUNICATION ENGINEERING)
REGULAR EXAMINATION, NOV- DEC 2016
2EC302 DIGITAL ELECTRONICS

TIME: 3 Hrs. TOTAL MARKS: 60

INSTRUCTION:
1. This question paper has two sections. Attempt each section in separate answer book.
2. Figures on right indicate marks.
3. Be precise and to the point in answering the descriptive questions.
4. Assume suitable data, if necessary.

SECTION-I

Q.1 (A) Find the following : 3
(i) 2's compliment of $(0.0110)_2$
(ii)10's compliment of $(25.639)_{10}$
(iii) 9's compliment of $(52520)_{10}$

(B) Prove following theorems of Boolean algebra : 3
(a) X + X = X
(b) X+1 = 1
(c) X(X+Y) = X

(C) Implement basic logic gates AND, OR and NOT using: 4
(a) NAND gates
(b) NOR gates

OR

Q.1 (A) Convert the following numbers from the given base to the bases indicated. 4
(a) Decimal 225.225 to binary, octal and hexadecimal.
(b) Binary 11010111.110 to decimal, octal and hexadecimal.
(c) Octal 623.77 to decimal, binary and hexadecimal.
(d) Hexadecimal 2AC5.D to decimal, octal and binary.

(B) Design a 3-bit odd parity generator circuit. 4

(C) Describe Exclusive - OR gate and Exclusive - NOR gate. 2

Q.2 (A) Express the following function in sum of minterms and product of maxterms. 4
(i) F(A,B,C,D) = D(A'+B) + B'D
(ii)F(W,X,Y,Z) = Y'Z + WXY' + W'X'Z + WXZ'

(B) Simplify the following Boolean function by using the tabulation method. 4
$F = \sum (0,1,2,8,10,11,14,15)$

(C) Design Half-adder circuit. 2

OR

Q.2 (A) Simplify using Karnaugh map: $F(A,B,C,D) = \prod(1,2,3,8,9,10,11,14)$. 4
Also implement it with minimum no. of NOR gates.

(B) Simplify the Boolean function using Karnaugh map: $F(A,B,C,D) = \sum(2,4,6,8,10)$, don't care condition $d = \sum(0,1,3)$. Draw the logic diagram from the derived Boolean expression. 4

(C) Design Half-Subtractor circuit. 2

Q.3 (A) Design a BCD to Excess-3 code converter circuit. 5

(B) Draw and explain the operation of 8x1 multiplexer. 3

(C) Give difference between Edge Triggering and Level Triggering. 2

SECTION-II

Q.4	(A)	Describe BCD adder with truth table and logic diagram.	5
	(B)	Give difference between decoder and demultiplexer. Draw and explain 3-to-8 line decoder.	5
		OR	
Q.4	(A)	Draw and explain 4-bit magnitude comparator.	5
	(B)	Describe programmable logic array (PLA).	5
Q.5	(A)	Draw logic diagram of JK Flip-flop and explain its working.	3
	(B)	Draw and Explain RTL basic NOR gate.	4
	(C)	Give difference between combinational circuit and sequential circuit with necessary block diagrams.	3
		OR	
Q.5	(A)	Draw logic diagram of D Flip-flop and explain its working.	3
	(B)	Draw and Explain DTL basic NAND gate.	4
	(C)	Explain Serial transfer of data from register A to B using shift register technique.	3
Q.6	(A)	Draw and Explain 4-bit Bidirectional Shift register with parallel load.	5
	(B)	Design 3-bit binary up counter using JK flip-flop.	5

END OF PAPER