Seat no._____

GANPAT UNIVERSITY

B. Tech. Semester IV Electronics & Communication Engineering Examination May-June 2012

2EC405 Digital Design using HDL

Max. Time: 2 Hrs.] **[Max. Marks: 35**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

1 **(A)** Draw and explain typical design flow for designing VLSI IC circuit. 3

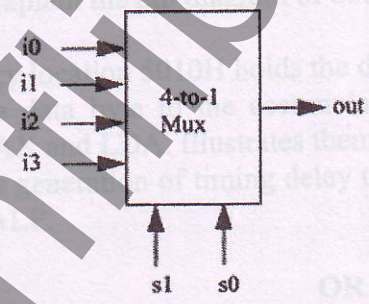
(B) Which are two possible styles of stimulus application? Explain each one with the help of suitable example. 3

(C) Explain `define, `include and `timescale compiler directive with help of example. 3

2 **(A)** Explain the following system tasks. 3

a. $stop
b. $fmonitor
c. $strobe
d. $readmemb
e. $fopen
f. $random

(B) Write a Verilog code for 4-to-1 multiplexer using gate primitive. 3



(C) What are the basic components of a module? Which components are mandatory? 3

OR

2 **(A)** Write a Verilog code for following digital circuits using continuous assignments. 3

a. 4 bit Binary to gray code converter
b. 4 bit Odd parity checker

(B) What would be the output/effect of the following statements? 3

a. latch = 4'd12;
$display("The current value of latch = %b\n", latch);
b. in_reg = 3'd2;
$monitor($time, " In register value = %b\n", in_reg[2:0]);
c. `define MEM_SIZE 1024
$display("The maximum memory size is %h", 'MEM_SIZE);

(C) Explain various types of gate delays with suitable example? 3

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SECTION-II

3 (A) Write a Verilog code for 4-bit ripple carry full adder by using 1-bit full adder. 3

(B) Compare and contrast. 3

a. initial block and always block.

b. continuous assignments and procedural assignments

(C) Evaluate output Y if A=4'b1100 , B=4'b1011 , C=4'b101x , D=4'b1001 2

1. Y= D + C
2. Y= ^B
3. Y= D >>> 1
4. Y = { 2{A} , 3{B} , C[0] , A[1] }

4 (A) Explain event based timing control in brief with the help of suitable example. 3

(B) Write a Verilog code for 8:3 encoder using casex statement. 3

(C) What are the differences between Task and Functions? 3

OR

4 (A) Write a Verilog code for 5 bit up-down counter and check its functionality with stimulus module. 3

(B) Explain different types of delay models. 3

(C) Explain following terms with examples. 3

a. assign and de-assign

b. Conditional compilation and conditional execution

End of Paper

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