Seat No.

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TOTAL MARKS: 70

GANPAT UNIVERSITY

B. Tech. Semester IV Electronics & Communication Engineering **Examination**, May-June 2012

2EC404 : Microprocessor Architecture & Programming

ain the 3-to-8 line decoder with logic diagram

TIME: 3 HOURS

INSTRUCTIONS:

0:3

- 1. Attempt all questions.
- 2. Answers to the two sections must be written in separate answer books.
- 3. Figures to the right indicate full marks.
- 4. Assume suitable data, if necessary.

SECTION-I

- Q:1 (A) Draw the timing diagram for execution of the instruction MVI A,54H 6
 - (B) Explain the generation of Read/Write control signals for I/O and Memory 6 with the help of schematic.

OR

Q:1 (A) Draw the memory classification diagram and explain each type in brief.

- (B) Draw and explain the pin diagram of 8085 microprocessor.
 - (A) The memory location 5010H holds the data byte 7FH. Write instructions to 6 0:2 transfer the data byte to the accumulator using three different opcodes: MOV, LDAX and LDA. Illustrates them with the help of block diagrams. 5
 - (B) Explain the generation of timing delay using one register with help of flow chart and ALP.

OR

(A) The memory location 3050H holds the data byte EEH. Write instructions 6 Q:2 to transfer the data byte to the accumulator using three different opcodes: MOV, LDAX and LDA. Illustrates them with the help of block diagrams. Explain the generation of timing delay using register pair with help of flow 5 **(B)** chart and ALP.

(A) List out & explain the Logical Instructions with the help of illustrations. Classify 8085 interrupts and explain them in brief. **(B)**

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SECTION-II

- Q:4 (A) What is the purpose of latch for microprocessor? Explain how control 5 signal MEMR, MEMW, IOW, IOR is generated. (B) Draw the memory chip address range of 4k (4096x8) with staring address 4 is 2000H.also specify last address. (C) Explain the 3-to-8 line decoder with logic diagram and functional table. 3 OR
 - Q:4 (A) Explain the operating system with hierarchical relationship between 5 computer hardware and software.
 - Draw the memory chip address range of 2k (2048x8) with staring address **(B)** 4 is B000H, also specify last address.
 - (C) Explain the concept of subroutine using CALL and RET instruction.
 - Q:5 (A) Draw the timing diagram for instruction IN 30H. Also calculate the total 7 time required for execution of this instruction when clock frequency is 2 MHz.
 - State differences between compiler and interpreter. **(B)**

OR

- Draw the timing diagram for instruction OUT 30H. Also calculate the 0:5 (A) 7 total time required for execution of this instruction when clock frequency is 6 MHz.
 - List out differences between machine language, assembly language and 4 **(B)** high-level language.
- 0:6

emsrgaib stems

- State and explain the function of 8237 in detail with block diagram. (A)
- State and explain the function of 8259 in detail with block diagram. **(B)**

End of Paper

MOV, LDAX and I.DA. Illustrates them with the slp of Explain the generation of timing delay using regist