Morning.
D:. 19/05/2014.

Seat no._____

GANPAT UNIVERSITY

B.Tech. EC Semester IV Regular Examination May/June-2014

2EC405 Digital design using HDL

Time: 2 Hrs.] [Total Marks: 35

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

1	(A)	Write a verilog code and it's test bench for 4-to-1 multiplexer using behavioral modeling.	4
	(B)	Write verilog code and it's test bench for 4 bit full adder using hierarchical modeling.	5
2	(A)	Draw and explain typical VLSI design flow.	4
	(B)	Write verilog code and test bench for 3 to 8 decoder using dataflow modeling style.	5
		OR	
2	(A)	Write a verilog code for following digital circuit: 1. JK Flip Flop 2. Up down counter	6
	(B)	Give the difference between initial and always with suitable example.	3

SECTION-II

3	(A)	Explain the looping statement with suitable example.	4
	(B)	Explain the system task with suitable example.	3
		OR	
3	(A)	Write a verilog code and test bench for NAND SR latch using gate level modeling.	3
	(B)	Give the difference between blocking and non blocking statement with suitable example.	4
4	(A)	Write a verilog code and test bench for 1:4 Demux using behavioral modeling.	5
	(B)	Write verilog code and it's test bench for ripple carry counter using hierarchical modeling	5

End of Paper