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D.: 23/05/2014.

GANPAT UNIVERSITY

B. Tech. Semester IV (EC)

CBCS Regular Examination May/June 2014

2 EC 404: Microprocessor Architecture & Programming

TIME: 3 HOURS] [TOTAL MARKS: 70

INSTRUCTIONS:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

Q:1 (A) Draw and explain the hierarchical relationship between computer hardware and software. 4

(B) List out and explain the Peripheral or Externally initiated operations. 4

(C) Tabulate 8085 Machine cycle status and Control signals 4

OR

Q:1 (A) Draw and explain the block diagram of Microprocessor Controlled Temperature System (MCTS) 4

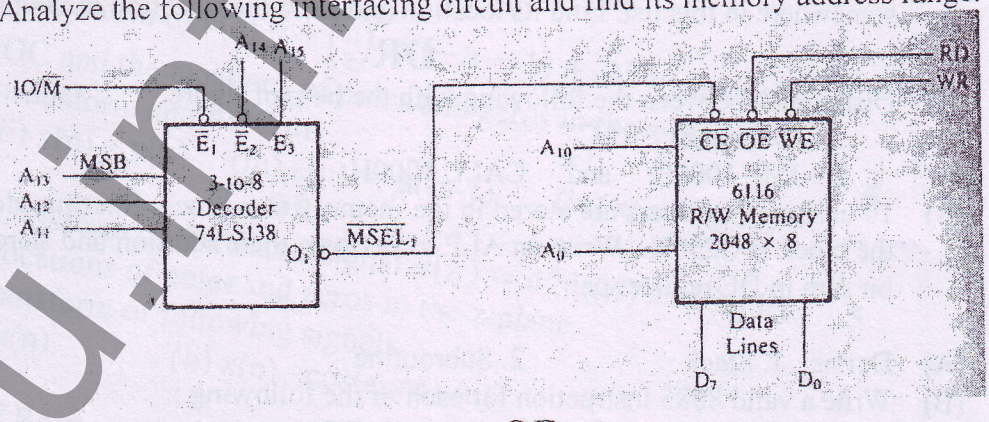
(B) Classify computer memory with the help of diagram. 4

(C) Draw the timing diagram of memory write cycle with appropriate example. 4

Q:2 (A) What is ALE? Draw the schematic of latching low-order address bus. 4

(B) Draw the timing diagram for execution of the instruction IN instruction. 4

(C) Analyze the following interfacing circuit and find its memory address range. 4



OR

Q:2 (A) Draw the structure with its requirements of typical memory chips. (i) R/W static memory (ii) EPROM. 4

(B) Draw the timing diagram for execution of the instruction OUT instruction. 4

(C) Explain the decoding logic and the memory address range of the 8155 shown in following figure. 4

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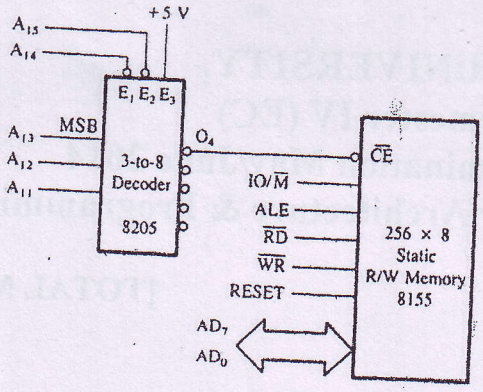

Q:3 (A) Draw and explain the timing diagram for execution of the STA 8000H. 6

(B) Design a seven-segment LED output port with the device address F5H, using a 74LS138 3-to-8 decoder, a 74LS20 4-input NAND gate, a 74LS02 NOR gate and a common-anode seven segment LED. 5

SECTION-II

Q: 4 (A) Tabulate the summary of Interrupts in 8085. 4

(B) Interpret the Accumulator Bit pattern for the SIM instruction. 4

(C) Explain how to handle multiple interrupts using a Priority Encoder? 4

OR

Q: 4 (A) Design a square wave generator with a pulse width of 100 μS by using the 8155 timer. Set up the timer in Mode 1 if the clock frequency is 3 MHz. 4

(B) List out the similarities and difference between the 8155 and 8255. 4

(C) Write a short note on 8155 I/O ports in Handshake mode. 4

Q: 5 (A) Explain following instructions in details with respect to Stack. 6

1. PUSH
2. SPHL
3. XTHL

(B) 15 unsigned numbers are stored in the memory as a list. List starts from the address C101H and ends at location C10FH. The number 17H is stored somewhere in this list. Find its location and store that location in DE pair. 5

OR

Q: 5 (A) Distinguish between the following with the help of figure. 6

1. RAL and RLC
2. JMP 1000H and CALL 1000H

(B) 10 unsigned numbers are stored in the memory as a block. Starting address of the block is C250H. Write an ALP to perform their addition and store the 16 bit sum in DE register pair. 5

Q: 6 (A) Define: 1. Stack 2. Subroutine 2

(B) Write a valid 8085 instruction for each of the following : 4

1. LDAX
2. STA
3. OUT
4. JP

(C) Write an ALP to count from 0F to 00H with a delay of 200 ms between each count. Count is displayed on PORT3. After the count 00H, the counter should reset itself and repeat the sequence. Use loop within loop concept for generating delay. Assume the system clock frequency to be 2Mhz. Suitable value of T-states should be considered while calculating delay. 6

End of Paper