GANPAT UNIVERSITY

B.Tech. EC Semester IV CBCS Regular Examination April-June-2015

2EC405 Digital Design using HDL

Time: 2 Hrs.] **[Total Marks: 35**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

Que:1	**(A)**	Explain the system task with suitable example.	**3**
	(B)	Write a verilog code and its testbench for 4-bit ripple carry counter using hierarchical modeling style.	**6**
		OR	
Que:1	**(A)**	Give the difference between blocking and non blocking assignment.	**4**
	(B)	Write a verilog code for 4 bit full adder using hierarchical modeling style.	**3**
	(C)	Give the difference between regular delay and intra assignment delay with suitable example.	**2**
Que:2	**(A)**	Write a verilog code & it's test bench for following digital circuit : 1. 3 to 8 decoder using if statement 2. D-latch using behavioral modeling style. 3. JK-Flipflop using case stament.	**6**
	(B)	Give the difference between initial block and always block with suitable example.	**2**

SECTION-II

Que:3	**(A)**	Write a verilog code for 4:1 Multiplexer using dataflow and behavioral modeling style.	**6**
	(B)	Give the difference between task and function with suitable example	**4**
		OR	
Que:3	**(A)**	Mention the work of following keywords. 1. $display 2. $monitor 3. Reg &wire	**4**
	(B)	Write a verilog code and its testbench for full substrator using gate level modeling style.	**6**
Que:4	**(A)**	Write a verilog code for upcounter using behavioral modeling style.	**4**
	(B)	Write a short note on looping statement.	**4**

End of Paper