Seat No:_____

GANPAT UNIVERSITY

B.Tech Semester V Electronics & Communication Engineering
CBCS Regular Examination November 2014
2EC504 Computer Organisation

Max. Time: 3 Hrs.] **[Max. Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

Que-1	(A)	What is the importance of bus in computer? List and briefly explain key elements of BUS design.	6
	(B)	What are the four main functions of a computer? Explain each with neat and clean diagram.	6
		OR	
	(A)	Draw instruction cycle state diagram. List and briefly define the possible states that define an instruction execution.	6
	(B)	Which factors affect the processor speed? Which three techniques are used to enhance the speed of processor? Explain each.	6
Que-2	(A)	Explain in detail hardwired implementation of a control unit.	6
	(B)	Which two techniques are used to replace block that is resident in the cache? Explain both techniques and list down its disadvantages.	5
		OR	
	(A)	For a direct-mapped cache, a main memory address is viewed as consisting of three fields. List and define the three fields. List down limitations of Direct mapping.	6
	(B)	Write the micro operations which are performed in fetch cycle and indirect cycle.	5
Que-3	(A)	What are the differences among positive overflow, exponent overflow, and significand overflow?	4
	(B)	What are the advantages of integrated circuit based system over transistor and vacuum tube based system?	4
	(C)	Draw and explain working of single bit Dynamic RAM structure.	4

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SECTION-II

Que-4 (A) List down different stages of six stage instruction pipelining. How these six stages improve performance of processor? Explain with help of timing diagram. 6

(B) What is the difference between direct instruction cycle and indirect instruction cycle? Explain with the help of block diagram. 6

OR

(A) Draw block diagram of two stage instruction pipelining. Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline? 6

(B) Which are the three types of pipelining hazards? Briefly explain resource hazard with the help of suitable example. 6

Que-5 (A) Draw and explain timing diagram of PCI read operation. 6

(B) Which steps are involved for the control of the transfer of data from an external device to the processor? Explain how I/O module communicates with the processor and with the external device. 5

OR

(A) Which three techniques are used for performing I/O? Briefly explain each technique. 6

(B) Briefly explain the Circular-Buffer Organization of Overlapped Windows. 5

Que-6 (A) List and briefly define the functional groups of signal lines for PCI. 4

(B) What are the differences between Large-Register-File Organizations and Cachc Organizations? 4

(C) Draw Generic Model of I/O Module and explain why I/O module required in computer system. 4

END OF PAPER