GANPAT UNIVERSITY

B. Tech. Semester VI (EC)
Regular Examination, May/June-2012

EC604 Digital Design Using HDL

Max. Time: 2 Hrs.] **[Total Marks: 35**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data if necessary

SECTION-I

1 (A) Explain following loops with suitable example: 4
   1. While
   2. For
   3. Forever
   4. Repeat

(B) Write a verilog program for 8:1 MUX using 5
   1. If.....else statement
   2. Case statement

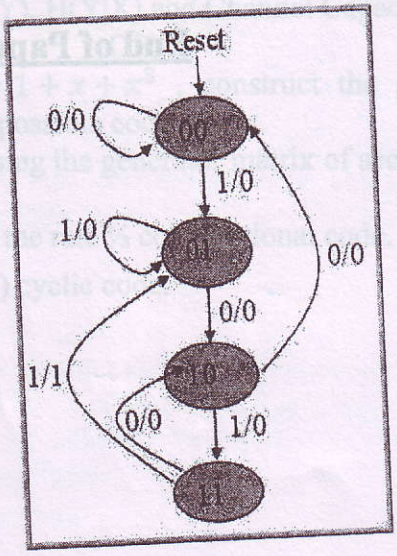
2 (A) Give the difference between task & function 5

(B) Write a verilog code for 4-bit unsigned up counter with asynchronous clear 4

OR

2 (A) Explain typical design flow to design VLSI chip in detail 3

(B) Write a verilog code for following FSM 6

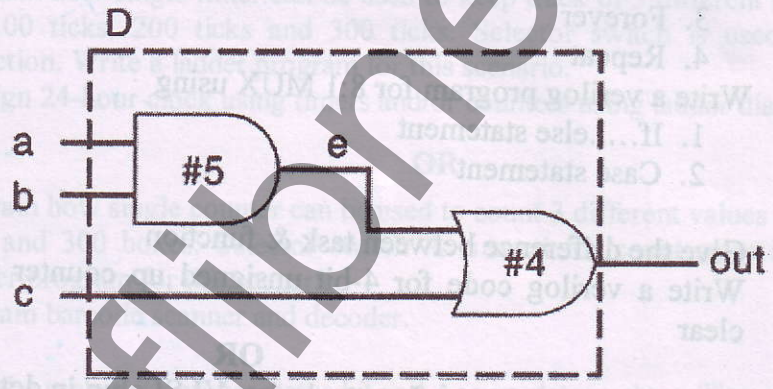


SECTION-II

3	(A)	Write a verilog code for 4-bit latch with an inverted gate and an asynchronous preset	5
	(B)	Give the types of delay based timing control with suitable example	4
4	(A)	Design verilog code for a circuit that calculates the Hamming distance of two 8-bit inputs.	4
	(B)	Explain the different system tasks and compiler directives with suitable example	4

OR

4	(A)	Write a verilog code to use as a serial to parallel converter	4
	(B)	Write a verilog code,testbench and draw the waveform for delay simulation for given below diagram	4



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