Seat No._____

GANPAT UNIVERSITY
B.TECH SEM.VII ELECTRONICS & COMMUNICATION ENGINEERING EXAMINATION, NOV/DEC-2011

EC 703 VLSI Technology

TIME: 3 Hrs.] **[TOTAL MARKS: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm,
$\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

SECTION-I

1	(A)	Draw the PLA implementation of following function : F1=XY+X'Z, F2=Y'+X'Z, F3=XY+Y'Z	6
	(B)	Draw the following CMOS based circuit : 1. 1 bit full adder. 2. D-Latch without using transmission gate.	6
		OR	
1	(A)	Design 4 input NAND Gate using pass transistor.	6
	(B)	Explain working principle of CMOS SRAM cell with necessary circuit diagram and waveforms for read and write operation.	6
2	(A)	What is lithography? List out the process steps for patterning silicon dioxide (SiO2).	6
	(B)	Using NORA implement the function AB+(C+D)+(EF+G).	6
		OR	
2	(A)	Explain channel length modulation for MOS transistor.	6
	(B)	Draw 4 stage carry look ahead adder using multiple output domino CMOS gate.	6
3	(A)	Consider a resistive-load inverter circuit with V_{DD}=5V, Kn'=20μA/V^2, V_{TO}=0.8V, R_L=200KΩ, and W/L=2. Calculate the V_{OL} and V_{IL} on the VTC.	5
	(B)	Draw the following digital circuit using Complementary Pass transistor logic 1. 2 input OR and NOR Gate 2. 2 input Ex-OR and Ex-NOR Gate	6

SECTION-II

4	(A)	Explain the types of MOSFET Capacitances.	6
	(B)	Explain following processes for the MOS system: 1. Accumulation 2. Depletion 3. Inversion	6

OR

4	(A)	Explain Gradual Channel Approximation (GCA) and derive equation for drain current I_D (lin) and I_D (sat).	6
	(B)	Explain all the four components of threshold voltage and derive equation of V_T in terms of V_{TO} and γ.	6
5	(A)	Optimize stick diagram layout of a complex CMOS logic gate Y=(AB+CD)'.	4
	(B)	Draw VLSI design flow (Y-chart).	4
	(C)	Draw the circuit diagram of a TSPC based rising edge-triggered DFF.	4

OR

5	(A)	What is DOMINO logic? Explain the concept of charge sharing.	3
	(B)	Write short notes on : Voltage bootstrapping.	6
	(C)	Draw the following digital circuit using transmission gate. 4:1 MUX using 2:1 MUX.	3
6	(A)	Explain working of three Transistor DRAM cell.	5
	(B)	Derive expression for depth of depletion region (Xd) and amount of charge in depletion region (Q) for two terminal MOS. Also find maximum depth of depletion region (Xdm).	6

End of Paper