Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Sem.VII (EC)

Regular Examination November/December-2012

EC702: DSP Architecture

Time: 3 Hours **Total Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Assume suitable data, if necessary.

SECTION-I

1	(A)	Explain Decimation process with examples.	3
	(B)	Why digital signal processors is require over general purpose processors.	4
	(C)	Explain interrupt handling by the processor using flow chart.	5
		OR	
1	(A)	Using 16 bits for the mantissa and 8 bits for the exponent, what is the range of numbers that can be represented using the floating point format similar to IEEE-754?	2
	(B)	What is the range of numbers that can be represented in a fixed point format using 8-bits & 16-bits if numbers are treated as (i) signed integers (ii) signed fractions.	3
	(C)	Explain interpolation process with examples.	3
	(D)	List out the difference between Microprocessor, Micro controller and DSP processor.	4
2	(A)	Explain the requirements of shifter in DSP processor.	6
	(B)	Design an interface to connect a 64 x 16 flash memory to a TMS320C54xx device. The processor address bus is A0-A15.	5
		OR	
2	(A)	Design a data memory system interface with address range 000800h – 000FFFh for a C5416 processor. Use 2K x 8 SRAM memory chips.	6
	(B)	Why barrel shifter required? How it work in DSP processor.	5
3	(A)	Explain McBSP of C54xx with block diagram.	6
	(B)	Difference between fixed point and floating point processor.	3
	(C)	Find the decimal equivalent of floating point binary number (i)1011000011100, (ii) 1111001011100. Assume the format similar to IEEE-754 in which the MSB is the sign bit followed by 4 exponent bits followed by 8 bits for fractional part.	3

SECTION-II

4 (A) Explain in brief von Neumann and Harvard bus architecture and why modified Harvard architecture is used in DSP processor. 5

(B) Explain the circular addressing mode. 2

(C) Explain the Q-notation. What values are represented by the 16-bit fixed point number N=4000h in the Q14 and Q8 notations? 5

OR

4 (A) Explain Direct Memory Access operation in DSP processor. 5

(B) Explain fixed point format for number representation in DSP implantations. 3

(C) Explain use of CPU status register bits MP/$\overline{MC}$, OVLY and DROM. 4

5 (A) Explain PMST register. 7

(B) Explain execution of instruction. Assume contents of register. 4

CMPS A, *AR4+

OR

5 (A) Explain memory mapped registers in brief. 7

(B) Explain execution of instruction. Assume contents of register. 4

MAC *AR5+, *AR6+,A, B

6 (A) Explain ST0 register of central processing unit. 7

(B) Write a short note on auxiliary register in DSP processor. 5

END OF PAPER