Seat no._____

GANPAT UNIVERSITY

B. Tech. Semester VII Electronics and Communication Engineering

Regular Examination NOV/DEC-2012

EC 703 VLSI Technology

Time: 3 Hrs.] **[Total. Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm,
$\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

SECTION-I

1	(A)	Explain Gradual Channel Approximation (GCA) and derive equation for drain current I_D (lin) and I_D (sat).	6
	(B)	Explain following processes for the MOS system with necessary diagram: 1. Accumulation 2. Depletion 3. Inversion	6

OR

1	(A)	Write a short note on MOSFET capacitance	6
	(B)	Draw the following CMOS based circuit : 1. CMOS implementation of the D-Latch 2. CMOS AOI realization of the JK latch	6
2	(A)	Give the types of voltage scaling and its effects on different parameters	6
	(B)	Draw the CMOS negative edge-triggered master slave D FF	5

OR

2	(A)	Implement (A+B)C using cascade domino CMOS logic	3
	(B)	Draw the following digital circuit using transmission gate 1. 2:1 MUX 2. 4:1 MUX 3. 2 input EX-OR gate 4. F=AB+A'C'+AB'C	8
3	(A)	Design 4 input NAND Gate using pass transistor	6
	(B)	What is latch up? Explain Causes of latch-up & how to avoid it.	6

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SECTION-II

4 (A) Explain CMOS ring oscillator circuit for three stages 6

(B) Calculate the threshold voltage V_{TO} at V_{SB}=0, for a polysilicon gate n-channel MOS transistor, with the following parameter: Substrate doping density $N_A=10^{16}$ cm^{-3} polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3},gate oxide thickness tox=500Å, and oxide-interface fixed charge density NOX = 4×10^{10} cm^{-2} 6

OR

4 (A) Give comparison of different inverter with necessary diagram. 4

(B) Explain channel length modulation effects in NMOS. 4

(C) Write a short note on voltage bootstrapping 4

5 (A) What is inverter threshold voltage? Explain its effect & derive the equation $\left(\frac{W}{L}\right)_P = 2.5\left(\frac{W}{L}\right)_N$ 6

(B) Draw circuit diagram of 3T DRAM cell with its working and related voltage waveforms. 5

OR

5 (A) Define τPHL & τPLH. Derive the equation for delay time(td) and explain its effect 4

(B) Draw the following digital circuit using transmission gate 4:1 MUX using 2:1 MUX 4

(C) Write a short note on LOCOS 3

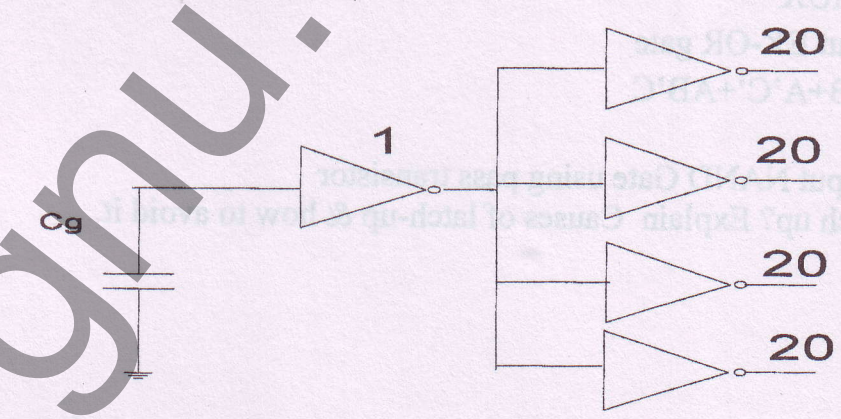
6 (A) Optimize stick diagram layout of a complex CMOS logic gate for Y=((A+B+C)D)' using Euler path method 6

(B) For given below circuit, if tpo=0.5ns then find delay for 6

(a) Non buffer case

(b) Single buffer case

(c) Super buffer case



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