Student Exam No._____

# GANPAT UNIVERSITY

## B. Tech. Semester VII Electronics and Communication Engineering

## CBCS Regular Examination December-2013

## 2EC703 VLSI TECHNOLOGY

**Time: 3 Hours** **Total Marks: 70**

**Instructions:**

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm, $\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

## SECTION-I

| | | | |
|---|---|---|---|
| 1 | (A) | Draw schematic and optimize stick diagram layout for following :<br>(1) Y=(A(D+E)+BC)'<br>(2) 4 input NAND gate | 6 |
| | (B) | Draw the following digital circuit using transmission gate :<br>(1) 4:1 MUX using 2:1 MUX<br>(2) F=AB+A'C'+AB'C | 6 |
| | | **OR** | |
| 1 | (A) | Draw the following CMOS based circuit :<br>(1) CMOS SR latch based on NOR2<br>(2) CMOS AOI realization of the JK latch | 6 |
| | (B) | Draw the following digital circuit using Complementary Pass transistor logic :<br>(1) 2 input AND and NAND gate<br>(2) Full adder | 6 |
| 2 | (A) | Draw the circuit diagram of a TSPC based rising edge-triggered DFF. | 5 |
| | (B) | Using NORA implement the function AB+(C+D)+(EF+G). | 6 |
| | | **OR** | |
| 2 | (A) | Draw 4 stage carry look ahead adder using multiple output domino CMOS gate. | 5 |
| | (B) | Explain the concept of charge sharing and explain the method of how to remove it. | 3 |
| | (C) | Implement (A+B)C using cascade domino CMOS logic. | 3 |
| 3 | (A) | Write a short note on CMOS ring oscillator | 6 |
| | (B) | Which are the two different VLSI design styles? How these design styles affect the design cycle time and circuit performance? Explain. | 6 |

## SECTION-II

4 (A) Write a short note on short channel effect. 6

(B) Explain MOSFET operation in linear and saturation with suitable diagram. 6

**OR**

4 (A) Write a short note on 6

(1) Narrow channel effect

(2) Constant field scaling

(B) Calculate the threshold voltage $V_{TO}$ at $V_{SB}=0$, for a polysilicon gate n-channel MOS transistor, with the following parameter: Substrate doping density $N_A=10^{16}$ $cm^{-3}$ polysilicon gate doping density $N_D = 2 \times 10^{20}$ $cm^{-3}$, gate oxide thickness tox=500Å, and oxide-interface fixed charge density $N_{OX} = 4 \times 10^{10}$ $cm^{-2}$ 6

5 (A) What is noise margin ? Define $V_{IH}, V_{IL}, V_{OL}, V_{OH}, V_{TH}$ 6

(B) Draw voltage transfer characteristics of CMOS inverter, identify critical voltage points and Find expressions of $V_{IL}$. 5

**OR**

5 (A) Draw voltage transfer characteristics of resistive load inverter, identify critical voltage points and Find expressions of $V_{OL}$. 6

(B) Consider the following for inverter design problem : 5

Given: VDD=5V, $kn'=30\mu A/V^2$ and VTO,n=1.0V,

Find the value of $R_L$ if W/L ratio is 2 and $V_{OL}=0.2V$.

6 (A) Explain working principle of CMOS SRAM cell with necessary circuit diagram and waveforms for read and write operation. 6

(B) Explain in detail latch-up. 6

**End of Paper**