Student Exam No._____

# GANPAT UNIVERSITY

## B.Tech. Semester VII Electronics and Communication Engineering

## CBCS Regular Examination November/December-2014

## 2EC703 VLSI Technology

**Max. Time: 3 Hrs.]** **[Total. Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm, $\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

## SECTION-I

| | | | |
|---|---|---|---|
| 1 | (A) | Explain working principle of CMOS SRAM cell with necessary circuit diagram and waveforms for read and write operation. | 6 |
| | (B) | Explain constant voltage scaling and its effects on different parameters. | 6 |
| | | **OR** | |
| 1 | (A) | Consider a resistive-load inverter circuit with $V_{DD}=5V$, $Kn'=20\mu A/V^2$, $V_{TO}=0.8V$, $R_L=200K\Omega$, and $W/L=2$. Calculate the $V_{OL}$ and $V_{IL}$ on the VTC. | 6 |
| | (B) | Draw the following digital circuit using Complementary Pass transistor logic :<br>1. 2 input OR and NOR Gat<br>2. 2 input Ex-OR and Ex-NOR Gate | 6 |
| 2 | (A) | What is latch up? How to avoid it. | 6 |
| | (B) | Explain the types of MOSFET Capacitances. | 5 |
| | | **OR** | |
| 2 | (A) | Draw the following CMOS based circuit :<br>1. CMOS SR latch based on NAND2<br>2. CMOS implementation of the D-Latch | 6 |
| | (B) | Implement (A+B)C using cascade domino CMOS logic | 5 |
| 3 | (A) | Using NORA implement the function AB+(C+D)+(EF+G). | 6 |
| | (B) | Draw and explain CMOS fabrication steps in brief. | 6 |

Student Exam No._____

## SECTION-II

| | | | |
|---|---|---|---|
| | (A) | Explain following processes for the MOS system:<br>1. Accumulation<br>2. Depletion<br>3. Inversion | 6 |
| | (B) | Explain Gradual Channel Approximation (GCA) and derive equation for drain current $I_D$ (lin) and $I_D$ (sat). | 6 |
| | | **OR** | |
| | (A) | Explain MOSFET operation in linear as well as in saturation region. | 6 |
| | (B) | List two VLSI design styles and compare them. | 6 |
| | (A) | Explain channel length modulation effects in NMOS. | 5 |
| | (B) | Calculate the threshold voltage $V_{TO}$ at $V_{SB}=0$, for a polysilicon gate n-channel MOS transistor, with the following parameter: Substrate doping density $N_A=10^{16}$ $cm^{-3}$ polysilicon gate doping density $N_D = 2 \times 10^{20}$ $cm^{-3}$, gate oxide thickness tox=500Å, and oxide-interface fixed charge density $N_{OX} = 4 \times 10^{10}$ $cm^{-2}$ | 6 |
| | | **OR** | |
| 5 | (A) | Optimize stick diagram layout of a complex CMOS logic gate Y= (A (D+E) +BC)' | 5 |
| | (B) | Draw the following digital circuit using transmission gate :<br>1. 2:1 MUX<br>2. F=AB+A'C'+AB'C | 6 |
| | (A) | Design 4 input NAND Gate using pass transistor. | 6 |
| | (B) | Draw the circuit diagram of a TSPC based rising edge-triggered DFF. | 6 |

**End of Paper**