Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester VII Electronics and Communication Engineering

Regular Examination November/December-2015

2EC703 VLSI Technology

Max. Time: 3 Hrs.] **[Total. Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm,
$\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

SECTION-I

1	(A)	Draw schematic and optimize stick diagram layout for following : 1. $Y=(A(D+E)+BC)'$ 2. 3 input NAND gate	6
	(B)	Using NORA implement the function AB+(C+D)+(EF+G).	6
		OR	
1	(A)	Explain the concept of charge sharing and explain the method of how to remove it.	6
	(B)	Implement (A+B)C using cascade domino CMOS logic.	6
2	(A)	What is noise margin? Define $V_{IH}, V_{IL}, V_{OH}, V_{OL}, V_{TH}$	5
	(B)	Draw the following digital circuit using transmission gate 1. F=AB+A'C'+AB'C 2. Two input EX-OR gate	6
		OR	
2	(A)	Explain MOSFET operation in linear and saturation with suitable diagram.	6
	(B)	Consider a resistive-load inverter circuit with V_{DD}=5V, $Kn'=20\mu A/V^2$, V_{TO}=0.8V, R_L=200KΩ, and W/L=2. Calculate the V_{OL} and V_{IL} on the VTC.	5
3	(A)	What is latch up? Causes of latch up and give the solution for how to remove latch up.	6
	(B)	Draw voltage transfer characteristics of CMOS inverter, identify critical voltage points and find expression of VIL.	6

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SECTION-II

4	(A)	Write a short note on : 1. LOCOS 2. STI	6
	(B)	Implement AB+(C+D)(E+F)+GH using domino CMOS logic.	6
		OR	
4	(A)	Draw the following digital circuit using Complementary Pass transistor logic 1. 2 input AND and NAND Gate 2. 2 input Ex-OR and Ex-NOR Gate	6
	(B)	Explain following processes for the MOS system : 1. Accumulation 2. Depletion 3. Inversion	6
5	(A)	What is lithography? List out the process steps for patterning silicon dioxide(SiO_2)	6
	(B)	Define following terms : 1. Punch through 2. DIBL and Sub threshold condition	5
		OR	
5	(A)	Design 4 input NAND Gate using pass transistor.	6
	(B)	Explain channel length modulation effects in NMOS.	5
6	(A)	Explain CMOS ring oscillator.	6
	(B)	Draw the following CMOS based circuit : 1. CMOS SR latch based on NAND2 2. CMOS implementation of the D-Latch	6

End of Paper