Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester VII Electronics and Communication Engineering

CBCS Regular Examination November/December-2016

2EC703 VLSI Technology

Max. Time: 3 Hrs.] **[Total. Marks: 70**

Instructions:

1. Attempt all questions.
2. Answers to the two sections must be written in separate answer books.
3. Figures to the right indicate full marks.
4. Use following data.

$\Phi_{F(gate)} = 0.55V$, $kT/q = 0.026V$, $q = 1.6\times10^{-19}$ C, $\epsilon_0 = 8.85\times10^{-14}$ F/cm, $\epsilon_{Si} = 11.7 \times \epsilon_0$ F/cm, $\epsilon_{ox} = 3.7 \times \epsilon_0$ F/cm, $n_i = 1.45 \times 10^{10}/cm^3$

SECTION-I

1	(A)	Draw and explain the steps in LOCOS process.	6
	(B)	Give the difference between CPLD and FPGA.	6
		OR	
1	(A)	Explain constant voltage scaling and its effects on different parameters.	6
	(B)	Explain the types of MOSFET Capacitances.	6
2	(A)	Explain Gradual Channel Approximation (GCA) and derive equation for drain current I_D (lin) and I_D (sat).	5
	(B)	Draw voltage transfer characteristics(VTC) of resistive load inverter, identify critical voltage points and find expressions of V_{OL}.	6
		OR	
2	(A)	Calculate the threshold voltage V_{TO} at $V_{SB}=0$, for a polysilicon gate n-channel MOS transistor, with the following parameter: Substrate doping density $N_A=10^{16}$ cm^{-3} polysilicon gate doping density $N_D = 2 \text{ X } 10^{20}$ cm^{-3}, gate oxide thickness t_{ox}=500Å, and oxide-interface fixed charge density $N_{OX} = 4 \text{ X } 10^{10}$ cm^{-2}	6
	(B)	Draw and explain CMOS fabrication steps in brief.	5
3	(A)	What is latch up? Causes of latch up and how to avoid it.	6
	(B)	Explain following processes for the MOS system: 1. Accumulation 2. Depletion 3. Inversion	6

SECTION-II

4	(A)	Optimize stick diagram layout of a complex CMOS logic gate Y= (A (D+E) +BC) '	6
	(B)	Draw the following digital circuit using transmission gate 1. 4:1 MUX 2. F=AB+A'C'+AB'C	6

OR

4	(A)	Implement (A+B) · C using cascade domino CMOS logic.	6
	(B)	Explain working principle of CMOS SRAM cell with necessary circuit diagram and waveforms for read and write operation.	6
5	(A)	Design 4 input NAND Gate using pass transistor.	6
	(B)	Explain channel length modulation effects in NMOS.	5

OR

5	(A)	Draw the following CMOS based circuit: 1. CMOS SR latch based on NAND2 2. CMOS implementation of the D-Latch	6
	(B)	Using NORA implement the function AB+(C+D) +(EF+G).	5
6	(A)	Draw the circuit diagram of a TSPC based rising edge-triggered DFF.	6
	(B)	Explain CMOS Ring oscillator.	6

End of Paper