Student Exam No: _____

GANPAT UNIVERSITY
B.TECH SEM-IV ELECTRICAL ENGINEERING
REGULAR EXAMINATION MAY / JUNE – 2014
2EE 401:- ANALOG AND DIGITAL ELECTRONICS

Time: 3 Hours **Total marks -70**

Instruction: - 1 Attempt all questions.
2 Make suitable assumptions wherever necessary.
3 Figures to the right indicate full marks.

SECTION – I

Q-1 (a) An n-p-n transistor at room temperature has its emitter disconnected. A voltage of 5 V is applied between collector and base. With collector positive, a current of 0.2 μA flows. When the base is disconnected and the same voltage is applied between collector and emitter, the current is found to be 20 μA. Find α, Base current, Emitter current When collector current is 1 mA. [6]

(b) List out the various methods used for transistor biasing. Explain Voltage Divider Bias Method. [6]

OR

Q-1 (a) Give constructional details of JFET and give its output characteristics. [4]
(b) Explain the IC – LM-317 with circuit diagram. [4]
(c) Explain the pin diagram of 555 timer IC. [4]

Q-2 (a) Draw a circuit diagram of practical differentiator using Op-Amp. Give the disadvantages of basic differentiator and explain if overcomes [5]

(b) Explain the Voltage Series Feedback Amplifier and also derive (i) closed loop voltage gain, (ii) Equation of Input Resistance. [6]

OR

Q-2 (a) Define following terms: [5]
(i) Slew Rate.
(ii) Common-Mode Rejection Ratio.
(iii) Supply Voltage Rejection Ratio.
(iv) Input Bias Current.
(v) Input Offset Current.

(b) Explain principle of Basic Comparator. Describe operation of Schmitt Trigger with necessary diagram. [6]

Q-3
(a) Explain the Voltage follower circuit of an Op-amp. [3]
(b) Define α and β. Show that : $\beta = \frac{\alpha}{1-\alpha}$ [3]
(c) What is an op amp ? Explain the Block diagram of an Op-amp. [3]
(d) Comparison between Open loop and Closed loop Configurations of Op-Amp. [3]

SECTION – II

Q-4 (a) Convert following. [6]

(i) $(7632)_8 = (?)_{10}$

(ii) $(35)_{10} = (?)_2$

(iii) $(11010101)_2 = (?)_8$

(iv) $(3509)_{10} = (?)_{16}$

(b) Explain AND, OR and NOT gates with electrical circuits and truth tables [6]

OR

Q-4 (a) (i) Using 1's complement method perform following binary subtraction. [6]

$(1011)_2 - (0111)_2$

(ii) Using 2's complement method perform following binary subtraction.

$(10110111)_2 - (11001110)_2$

(b) Comparison between combinational and sequential circuit. [4]

(c) Prove Following: [2]

$A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$

Q-5 (a) Explain 8 to 1 multiplexer with bock diagram, truth table and logic circuit. [5]

(b) Find out POS for following function. [4]

$f(A,B,C) = (A + B)^* (A + \bar{B})^* (\bar{B} + \bar{C})$

(c) Give the full name of BCD and ASCII codes. [2]

OR

Q-5 (a) Explain J-K flip flop with necessary diagram and truth table. [4]

(b) Find out SOP for following function. [4]

$f(A,B,C,D) = AB\bar{C} + A\bar{B} + \bar{A}C$

(c) Simplify following function using k-map. [3]

$f(A,B,C,D) = \sum m(1,4,6,8,9,10,11)$

Q-6 Answer the following question. (Any three) [12]

(a) Explain EX-OR and EX-NOR gates with electrical circuits and truth tables

(b) Explain T flip flop with necessary diagram and truth table.

(c) Draw the half adder circuit and explain it by using their truth table.

(d) Explain De-Morgan's theorem with logic gates and truth tables.

END OF PAPER