Student Exam No:-_____

GANPAT UNIVERSITY
B.TECH SEM-IV (ELECTRICAL)
REGULAR EXAMINATION APRIL-JUNE 2016
2EE403: DIGITAL ELECTRONICS & MICROPROCESSOR

Time: 3 Hours **Total Marks:-60**

Instructions: - 1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

SECTION-I

Que.-1 **(A)** Perform the following arithmetical operations: **[06]**

(i) $(679.6)_{BCD} + (536.8)_{BCD}$, (ii) $(687)_{XS-3} - (348)_{XS-3}$(use 9's compliment method)

(B) (i) $(1101.11)_2 \times (101.1)_2$=_____, (ii) $(105.15)_{10} = (?)_2$ **[04]**

OR

Que.-1 **(A)** (i) 2928.54 - 416.7 = (?) (using 10's compliment method) **[06]**

(ii)Convert $(378.93)_{10}$ to octal

(B) Define the following terms: **[04]**

(i) XS-3 code (ii) ASCII code (iii) double dabble method.(iv)BCD code

Que.-2 **(A)** Draw the circuit diagram of an edge triggered JK flip flops with 'active low preset' and 'active low clear' using NAND gates and explain its operation with the help of truth table. **[05]**

(B) Write a short note on two bit ripple up & down counter using negative edge – triggered flip flops. **[05]**

OR

Que.-2 **(A)** Explain the positive edge triggered transparent & toggle flip flops along with its truth tables. **[05]**

(B) With neat sketch, design 4-bit Parallel in, Serial out type shift register. **[05]**

Que.-3 **Attempt any Two:** **[10]**

(A) Draw the circuit diagram of a master-salve D Flip flop and explain its operation with the help of a truth table. How is it different from edge triggering?

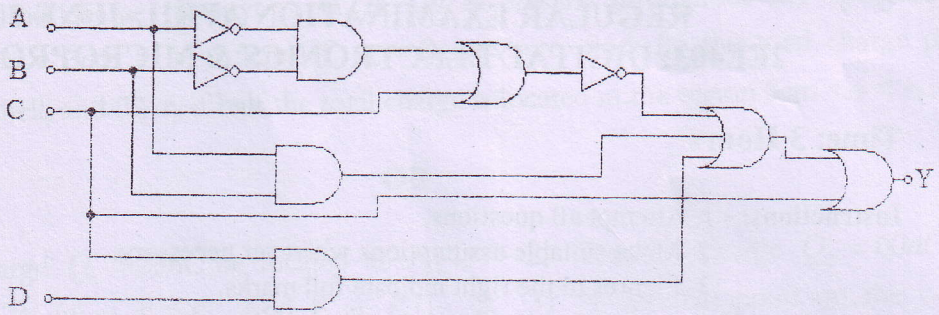
(B) (i) What is UART?

(ii) Explain the working of 4-bit buffer register.

(C) Explain half adder and full adder in detail.

SECTION-II

Que.-4 (A) Write the Boolean expression for the logic diagram given below and simplify it as much as possible and draw the logic diagram that implements the specified reduced expression. [04]



(B) Expand F= (x+yz)' to min term and max term. [02]

(C) State and prove De Morgan's theorem. [04]

OR

Que.-4 (A) Prove that: [05]

a. A'(A+B)+[(B+AA)(A+B')]= A+B

b. AB'+A(B+C)'+B(B+C)'= AB'

(B) Reduce the expression F= $\sum$m (0, 3, 4, 6, 7, 9, 12, 14, 15) using mapping and implement the reduced expression in logic diagram. [03]

(C) Show that AOB = AB+ A'B' = (AB'+A'B)' [02]

Que.-5 (A) What are the various registers of 8085? Discuss their function. Also discuss status flags of 8085. [05]

(B) Classify memory and explain demultiplexing of AD7 to AD0 in detail. [05]

OR

Que.-5 (A) Explain function of following instruction with suitable example. [06]

1. LHLD addr
2. XCHG
3. ACI data
4. MOV r, M
5. ANA M
6. JNC addr

(B) Discuss various types of addressing modes of 8085 with suitable example. [04]

Que.-6 **Attempt any two:** [10]

(A) Write a program to find square of a number from 0 to 9 using lookup table.

(B) Write a program to add 16, 2B, 39 and 12 H. Numbers are placed in the memory locations 2501 to 2504 H and store the result in the memory location 2450 H.

(C) Write an ALP to arrange a series of numbers in descending order.

END OF PAPER