Student Exam No: _____

GANPAT UNIVERSITY

B.TECH SEM. IV - MECHATRONICS ENGINEERING

CBCS REGULAR EXAMINATION MAY/JUNE - 2012

2MC403 DIGITAL CIRCUITS & DEVICES

Time: 3 Hours **Total Marks: 70**

Instructions:

1). All questions are **compulsory**.
2). Figures to the **right** indicate full marks.
3). Answers to the two sections must be written in **separate** answer books.
4). Assume all necessary data.

Section – I

Que:-1 **Attempt All.** **[12]**

(A) Make a K map of the following expression and obtain the minimal SOP and POS forms.

AB + AC' + C + AD + AB'C + ABC

(B) Expand A (A + B') B to maxterms and minterms.

(C) Explain ROM.

OR

Que:-1 **Attempt All.** **[12]**

(A) Design a combinational circuit that has accepts a 3 bit BCD number and generates an output binary number equal to the square of the input number.

(B) Prove that A[B + C'(AB + AC)'] = AB.

(C) Draw the logic diagram for full adder using NAND logic and NOR logic.

Que:-2 **(A)** Solve by tabulation method. **[06]**

$F(A, B, C, D) = \sum(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$.

(B) Design BCD to Decimal decoder. **[05]**

OR

Que:-2 **(A)** Solve by tabulation method. **[06]**

$F(A, B, C, D) = \sum(0, 1, 2, 8, 10, 11, 14, 15)$.

(B) Design octal to binary Encoder. **[05]**

Que:-3 **Attempt All.** **[12]**

(A) Implement the following function with a multiplexer.

$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 13, 15)$

(B) 1. Draw the switching circuit for (A + B)(C + D).
2. Explain self complemented codes.

(C) 3. Do the subtraction using 1's compliment.
0100-101111= _____
4. Do base conversion for following.
$(420)_{10}$ = (_____)$_8$

Section – II

Que:-4 Attempt All. **[12]**

(A) Explain the DTL logic.
(B) Explain D type negative edge triggered flip flop with logic diagram.
(C) Explain successive-approximation A/D converter.

OR

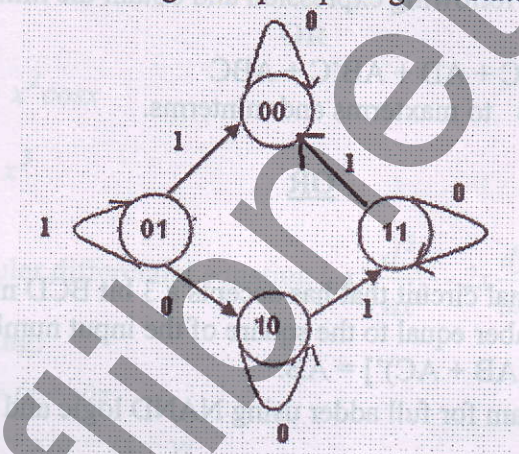
Que:-4 Attempt All. **[12]**

(A) Draw the inverter, NAND gate and NOR gate using CMOS logic.
(B) Give the difference between sequential and combinational circuits.
(C) Explain DAC.

Que:-5 (A) Design the counter that repeat the seequance of 0, 1, 2, 4, 5, 6 using JK flip- flop. **[06]**
(B) Explain 4 bit binary ripple counter. **[05]**

OR

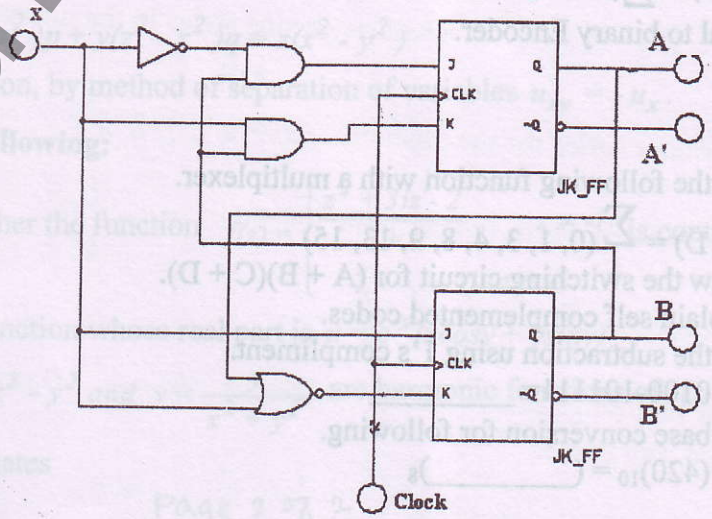
Que:-5 (A) Design the sequential Circuit using JK flip-flop for given state diagram **[06]**



(B) Explain BCD counter. **[05]**

Que:-6 Attempt All. **[12]**

(A) Explain the conversion of D flip-flop to RS flip flop.
(B) Draw the logic diagram for 4 bit bidirectional shift register with parallel load.
(C) Prepare state table and state diagram for the following sequential circuit with JK flip- flop.



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