Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester: IV Mechatronics Engineering

Regular Examination May 2014

2MC403 DIGITAL CIRCUITS & DEVICES

Time: 3 Hours **Total Marks: 70**

Instruction:

1). All questions are **compulsory.**
2). Figures to the **right** indicate full marks.
3). Answers to the two sections must be written in **separate** answer books.
4). Assume all necessary data.

Section - I

Que. – 1	**Attempt all.**		**12**
	A	Design an 8 to 1 line multiplexer.	4
	B	Solve following:	4
		1. $x + x = x$	
		2. $x + 1 = 1$	
		3. $(x + y)' = x'.y'$	
		4. $x + x.y = x$	
	C	Design a BCD to decimal decoder.	4
		OR	
Que. – 1	**Attempt all.**		**12**
	A	Implement the following function by MUX.	4
		$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$	
	B	Design and explain a 4 bit BCD adder.	4
	C	Solve the following by tabulation method & compare answer with K-map.	4
		$F(A, B, C, D) = \sum (0, 1, 2, 8, 10, 11, 14, 15)$	
Que. – 2	**Attempt all.**		**11**
	A	Design and explain Excess 3 to BCD code converter using MSI.	4
	B	Discuss the various types of logic gates in detail.	4
	C	Explain the concept of priority encoder.	3
		OR	
Que. – 2	**Attempt all.**		**11**
	A	Discuss the concept of carry propagation and solution for the same.	4
	B	Explain 4-bit binary to grey code converter.	4
	C	Design a half subtractor circuit.	3
Que. – 3	**Attempt all.**		**12**
	A	Design & explain magnitude comparator.	4
	B	Design & implement a full adder with its implementations.	4
	C	Simplify the following Boolean function using K-map.	4
		$F(A, B, C, D, E) = \sum (0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$	

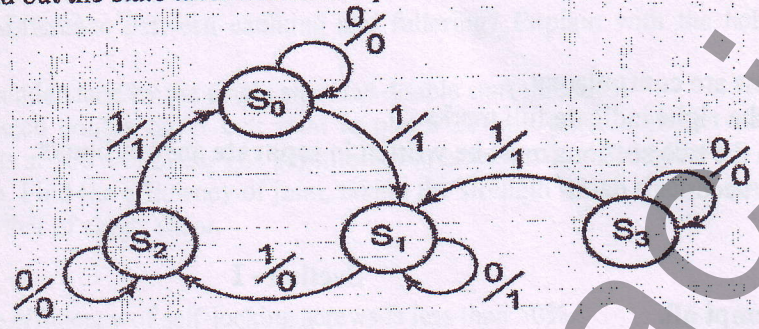
Section – II

Que. – 4 **Attempt all.** 12

A With the use of the excitation table carry out the following conversion: 6

1. SR to JK
2. SR to D
3. T to JK
4. D to SR

B Find out the state table and state equations for the figure. 6

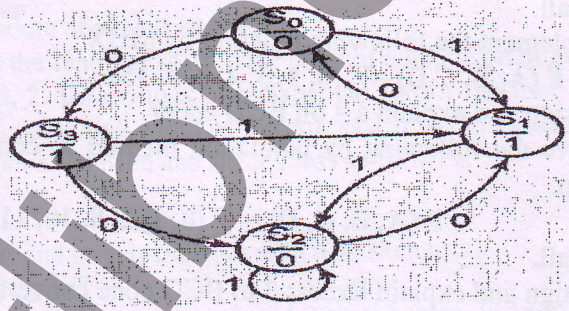


OR

Que. – 4 **Attempt all.** 12

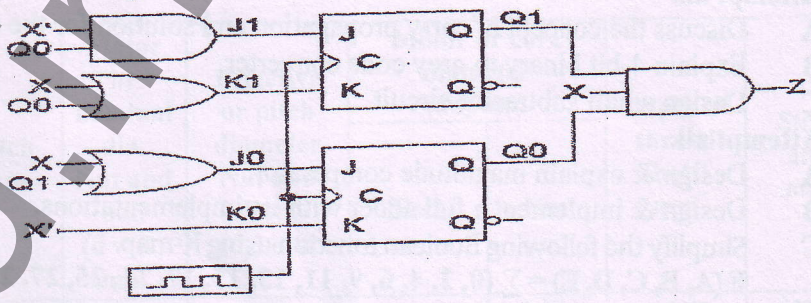
A Design the binary counter having the following repeated sequence 0,1,3,2,6,4,5,7 continuously. Use RS flip flop. 6

B Find out the state table and state equations for the figure. 6



Que. – 5 **Attempt all.** 11

A Do the analysis of the circuit given in figure. 6



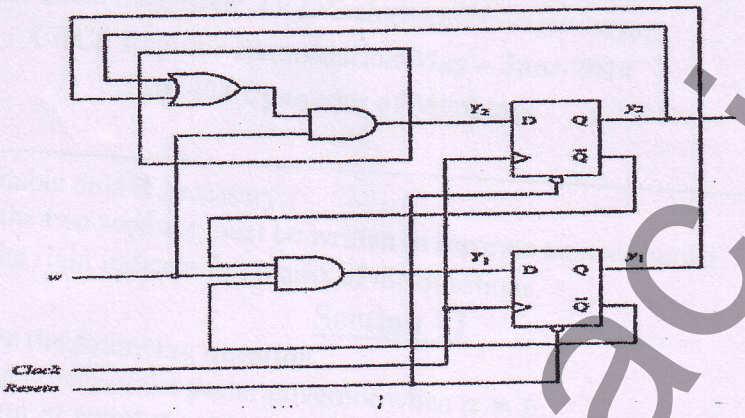
B A sequential circuit with two *D* flip-flops, *A* and *B*; two inputs, *x* and *y*; and one output, *z*, is specified by the following next-state and output equations: 5

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA$$
$$z = B$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

Que. – 5 **Attempt all.** **11**

A Do the analysis of the circuit given in figure. **6**



B A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x*. The circuit is described by the following flip-flop input equations: **5**

$$J_A = x \qquad K_A = B'$$
$$J_B = x \qquad K_B = A$$

(a) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the *J* and *K* variables.
(b) Draw the state diagram of the circuit.

Que. – 6 **Attempt all.** **12**

A **6**

1. Convert $(325)_8$ to decimal.
2. Convert $(78)_{10}$ to binary number.
3. Perform subtraction using 1's compliment.
   $(1010100)_2$-$(1000011)_2$

B PN flip flop has four operations, no change, clear to 0, set 1 and compliment, when inputs P and N are 00,01,10 and 11 respectively. **2**

1. Draw excitation table and truth table
2. Derive the characteristic equations.

C Reduce the number of states in the following state table and tabulate the reduced state table **4**

Present state	Next state x=0	Next state x=1	Output x=0	Output x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

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