Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester: IV Mechatronics Engineering

Regular Examination April – June 2015

2MC403 Digital Circuits & Devices

Time: 3 Hours **Total Marks: 70**

Instruction: 1 All questions are compulsory.
2 Specify assumptions made in answer sheet (if needed only).
3 Draw diagrams and tables neat and clean.

Section - I

Que. 1 **Attempt the following.**

(a) Design a sequential circuit which produces output '1' if inputs are greater or equal to previous inputs. Assume two bits of input. Use JK flip-flops. [6]

(b) Perform BCD addition operation of two numbers: $(95)_{10}$ and $(05)_{10}$. [3]

(c) Using r's and (r-1)'s compliment method, find out compliment of $(C3DF)_{16}$. [3]

OR

Que. 1 **Attempt the following.**

(a) Draw logic circuit diagram, state table and state diagram for following state equations. [6]

$$A(t+1) = x(y' + B)$$
$$B(t+1) = x(A + B')$$
$$z = A$$

(b) Determine the base in each case for the following operations to be correct. [3]

I. 14/2=5
II. 24+17=40

(c) Express the following numbers to decimal. [3]

I. $(16.5)_{16}$
II. $(26.24)_{8}$

Que. 2 **Attempt the following.**

(a) Explain SR Latch with circuit and function table. [4]

(b) Draw a four bit shift register circuit diagram and explain its working. [3]

(c) Draw and explain four bit ripple counter with D flip-flop. [4]

OR

Que. 2 **Attempt the following.**

(a) Explain serial adder circuitry with circuit diagram. [4]

(b) What is the functional difference between D flip-flop, T flip-flop and JK flip-flop? Elaborate your answer with help of examples. [3]

(c) Draw and explain four bit ripple counter with JK flip-flop. [4]

Que. 3 **Attempt ALL.** [12]

(a) Write a short note on ASCII and error detection codes.

(b) The initial content of four bit shift register is 1101. The input to the shift register is 1010111. If the content of shift registers is shifted right for six times, what will be its content at each instance?

(c) Design a BCD synchronous counter.

Section – II

Que. 4 **Attempt the following.**

(a) Design and explain a circuit to add two 4 bit BCD numbers. [4]

(b) Design and explain a 4 to 1 line MUX. [4]

(c) Solve by K-map. [4]

$$F(Q, W, E, R, T) = \Sigma (0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$$

OR

Que. 4 **Attempt the following.**

(a) Design and explain a circuit to add two bits with its implementations. [4]

(b) Design and explain quadruple 2 to 1 line multiplexer. [4]

(c) Simplify the following Boolean function using k-map & find answer in SOP & POS. [4]

$$F(j, a, c, k) = \sum (0, 1, 2, 5, 8, 9, 10)$$

Que. 5 **Attempt the following.**

(a) Solve by tabulation method and compare your answer with K-map. [6]

$$F(A, B, C, D) = \Sigma (1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$$

(b) Design & explain 4 bit binary to grey code converter using SSI circuit. [5]

OR

Que. 5 **Attempt the following.**

(a) Design & explain the Binary parallel adder with look ahead carry generator. [6]

(b) Design & explain the circuit for comparison between two 4 bit binary. [5]

Que. 6 **Attempt ALL.** [12]

(a) Design and explain Full adder with two decoders and OR gates.

(b) Design and explain 4 bit BCD to decimal decoder.

(c) Write a short note on DTL.

(d) Implement an Ex-OR gate only with NAND gates.

END OF PAPER