Exam No: _____

GANPAT UNIVERSITY

B. TECH SEM-IV (Mechatronics) REGULAR EXAMINATION– APRIL-JUNE 2016

2MC401: Digital Circuits & Devices

TIME: 3 HRS **TOTAL MARKS: 60**

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Q. 1		**Attempt all.**	(10)
	(A)	Design and explain 4 bit adder for addition of two BCD numbers.	(04)
	(B)	Design and explain 4 bit Magnitude Comparator.	(04)
	(C)	Prove the Distributive law and De Morgan's law.	(02)

OR

Q. 1		**Attempt all.**	(10)
	(A)	Design a 4 bit binary to grey code converter using SSI.	(04)
	(B)	Design a BCD to Excess 3 code converter with a BCD to decimal decoder and four OR gates.	(04)
	(C)	Design a Full adder with two 3 x 8 decoders and OR gates	(02)
Q. 2		**Attempt all.**	(10)
	(A)	Design an 8 to 1 line Multiplexer.	(04)
	(B)	Design a binary parallel adder and explain the solution for the carry propagation delay time.	(04)
	(C)	Reduce the following Boolean function to the required number of literals. **[(CD)' + A]' + A + CD + AB** to three literals.	(02)

OR

Q. 2		**Attempt all.**	(10)
	(A)	Design and explain a quadruple 2 to 1 line multiplexer.	(04)
	(B)	Solve by tabulation method. **F (R, S, T, U) = Σ (1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)**	(04)
	(C)	Reduce the following Boolean function to the required number of literals. **(A +C +D)(A +C +D')(A +C' + D)(A + B')** to four literals.	(02)
Q. 3		**Attempt All.**	(10)
	(A)	Design and explain a circuit to add two bits with its implementations.	(03)
	(B)	Solve by K-map. **F (T, R, A, C, E) = Σ (0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)**	(03)
	(C)	Design and explain a 4 x 16 decoder with two 3 x 8 decoders.	(04)

SECTION: II

(10)

Q. 4 **Attempt all.**

(A) Explain in detail all the logic gates used in digital circuits. (04)

(B) Write a short note on RTL. (04)

(C) Explain the characteristics of IC digital logic families. (02)

OR

(10)

Q. 4 **Attempt all.**

(A) Discuss in detail the standard design procedure of designing a combinational circuit with example. (04)

(B) Write a short note on DTL. (04)

(C) Draw the logical circuit for **F= AB + CD + E** using NAND gates only. (02)

(10)

Q. 5 **Attempt all.**

(A) **Solve the following conversion.** (06)

1.Octal to Decimal	(a) 4057.06	(b) 724.32
2.Decimal to Binary(Using Double Dabble)	(a) 163.875	(b) 105.15
3.Octal to Hexadecimal	(a) 657.603	(b) 678.320

(04)

(B) **Solve the following.**

1. Add +40.75 to - 40.75 using 12 bit 2's complement.
2. Represent -99 and -77.25 in 8 bit 1's complement.

OR

(10)

Q. 5 **Attempt all.**

(A) **Differentiate the following.** (06)

1.Sequential circuits and Combinational circuits

2.Synchronous and Asynchronous circuits

(B) **Solve the Followings.** (04)

1. Add -47.25 to +55.75 using 2's complements.
2. Express -73.75 in 12 bit 2's complements form.

(10)

Q. 6 **Attempt All.**

(A) Explain the digital computer with block diagram. (03)

(B) Design and explain J-K flip flop. (03)

(C) Explain the R – S flip flop with logical circuit diagram. (04)

END OF PAPER