Exam No: _____

GANPAT UNIVERSITY

B. TECH SEM- IV (MC) CBCS REGULAR EXAMINATION– APRIL-JUNE 2017

2MC401: Digital Circuits & Devices

TIME: 3 HRS TOTAL MARKS: 60

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.

SECTION: I

Q.1

A. Reduce the following Boolean functions to the given number of literals. **(04)**

1. **[(CD)' + A]' + A + CD + AB** to three literals.
2. **(A + C + D)(A + C + D')(A + C' + D)(A + B')** to four literals.

B. Design & explain a half subtractor with its implementations. **(04)**

C. Explain the various characteristics of IC digital logic family. **(02)**

OR

Q.1

A. Design & explain the Full Adder with its implementations. **(04)**

B. Design & explain the 4 bit BCD to decimal decoder. **(04)**

C. Implement following: **(02)**

1. An Ex-OR gate by NAND gates only.
2. **F(A,B,C,D,E) = (A + B) *(C + D) *E** by NOR gates only.

Q.2

A. Design & explain 4 bit BCD to Excess-3 code converter using SSI circuit. **(04)**

B. Solve by K-map. **(04)**

F (Q, W, E, R, T) = Σ (0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)

C. Implement the following function with a multiplexer. **(02)**

F (A,B,C) = ∑ (1, 3, 5, 6)

OR

Q.2

A. Design & explain the 4 bit BCD Adder with an example. **(04)**

B. Design and explain quadruple 2 to 1 line multiplexer. **(04)**

C. Implement the following function with a multiplexer. **(02)**

F (A,B,C,D) = ∑ (0, 1, 3, 4, 8, 9, 15)

Q.3

A. Design & explain the 4 bit magnitude comparator.

B. Solve by tabulation method and compare your answer with K-map.

$F(Z, X, C, V) = \Sigma (0, 2, 3, 6, 7, 8, 9, 10, 13)$

SECTION: II

Q.4

A. Explain the DTL digital logic family. (04)

B. List out different binary codes and differentiate weighted and non- weighted binary codes. (03)

C. Do as Directed. (03)

1. Convert the base: $(628)_8 = (\_\_\_\_\_)_{16}$
2. Do the subtraction using 2's compliment: $100011 - 1101 = \_\_\_\_\_$

OR

Q.4

A. Draw the logical diagram of 4 x 3 RAM. (04)

B. Draw the circuits for Inverter, NAND gate and NOR gate using NMOS logic. (03)

C. Do as Directed. (03)

1. Convert the base: $(128)_{10} = (\_\_\_\_\_)_2$
2. Do the BCD addition: $864 + 238 = \_\_\_\_\_$

Q.5

A. Explain 4 bit BCD ripple counter. (04)

B. Design 3 bit Binary counter using T flip flop. (04)

C. Draw the logic diagram for 3 bit shift register. (02)

OR

Q.5

A. Explain the 4 bit register with parallel load compatibility using D flip flop. (04)

B. Design a serial adder using a sequential logic procedure. (04)

C. Give the differences between 1's and 2's complement. (02)

Q.6 (10)

A. Explain D flip flop and master slave flip flop.

B. Design the sequential circuit with JK flip- flop to satisfy the following state equations:

$A(t + 1) = A'B'CD + A'B'C + ACD + AC'D'$
$B(t + 1) = A'C + CD' + A'BC'$
$C(t + 1) = B$
$D(t + 1) = D'$

----------END OF PAPER----------