Student Exam No: _____

GANPAT UNIVERSITY

B.TECH SEM. V - MECHATRONICS ENGINEERING
REGULAR EXAMINATION NOV/DEC - 2011
MC-505 MICROPROCESSOR

Time: 3 Hours **Total Marks: 70**

Instructions:

1). All questions are **compulsory**.
2). Figures to the **right** indicate full marks.
3). Answers to the two sections must be written in **separate** answer books.
4). Assume all necessary data.

Section – I

Que:-1 Attempt All. **[12]**

(A) Explain the assembly language of the 8085 microprocessor.
(B) List the four operations commonly performed by the 8085 and explain how are they performed by the 8085.
(C) Design a SRAM chip for the address range 4888H to CFFFH.

OR

Que:-1 Attempt All. **[12]**

(A) Explain different components of 8085 microprocessor based system.
(B) (i) If the memory chip size is 1024 x 4 bits, how many chips are required to make up 16 K bytes of memory?
(ii) Explain the difference between SRAM vs. DRAM.
(C) Explain different control and status signals of the 8085 microprocessor.

Que:-2 **(A)** Two machine codes- 0001 0110 (16H – MVI C) and 0100 0010 (42H) – are stored in memory locations C500H and C501H, respectively. Illustrate the bus timings as these machine codes are executed. Calculate the time required to execute the Opcode Fetch and the Memory Read cycles and the entire instruction cycle if the clock frequency is 3 MHz. **[08]**

(B) Explain the difference between the absolute and partial decoding. **[03]**

OR

Que:-2 **(A)** Design a seven-segment LED output port with the device address F3H using a 74LS138 3-to-8 decoder, a 74LS20 4-input NAND gate, a 74LS02 NOR gate and a common-anode seven-segment LED. Write instructions to display 5 at the port. **[08]**

(B) Define machine cycle, instruction cycle and T-state. **[03]**

Que:-3 Attempt Any Three. [12]

(A) Explain difference between peripheral mapped I/O and memory mapped I/O.
(B) Draw the timing diagram for IN 55H instruction.
(C) Explain demultiplexing the address bus and data bus.
(D) Explain the 8085 vectored interrupts.

Section – II

Que:-4 Attempt All. [12]

(A) A set of eight data bytes is stored in memory locations starting from C070H.Write a program to add two bytes at a time and store the sum in the same memory locations, low-order sum replacing the first byte and a carry replacing the second byte. If any pair does not generate a carry, the memory location of the second byte should be cleared.
(B) Write an ALP to generate a rectangular wave of 15 ms of ON period and 31 ms OFF period on bit D7 of output port 05H.
(C) Write an ALP to generate 1 KHz square wave from counter 1 of 8254.

OR

Que:-4 Attempt All. [12]

(A) A set of ten bytes is stored in memory starting with the address C050H. Write a program to check each byte, and save the bytes that are higher than 40_{10} and lower than 100_{10} in memory locations starting from C060H.
(B) Write an ALP to generate a rectangular wave of 51 ms of ON period and 103 ms OFF period on bit D1 of output port 05H.
(C) Write an ALP to generate 10 KHz square wave from counter 0 of 8254.

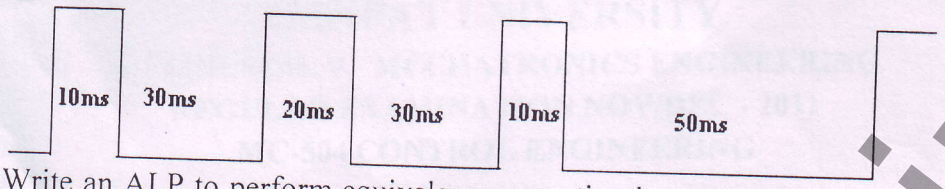
Que:-5 (A) Draw the block diagram of 8254 and Write an ALP to provide given ON/OFF time to three traffic lights and two pedestrian Signs (WALK and DON'T WALK) connected to pin of the Port C of 8255 as shown below. Use 8254 for delay. [08]

Light	Pin	On time
Green	PC3	10 Sec.
Yellow	PC4	5 Sec.
Red	PC5	15 Sec.
WALK	PC6	10 Sec
DON"T WALKS	PC7	20 Sec

(B) Write an ALP to add two number store in memory location C200H and C201H. Store the result in memory location C300H (lower byte) and C301H (higher byte). [03]

OR

e:-5 **(A)** Draw the block diagram of 8255 and Write an ALP to generate the following waveform on the output pin 3 of the port C of 8255. Use 8254 for delay. **[08]**



(B) Write an ALP to perform equivalence operation between content of register B and C. store result in memory location C500H. **[03]**

Que:-6 **Attempt All.** **[12]**

(A) Write an ALP to complement the even bit of the register C without using CMA instruction.(even bit means D0, D2, D4, D6 bit of Register C)

(B) Calculate the delay for the following instructions:

```
Loop 2: MVI E, 38H
        MVI D, FFH
Loop 1: DCR D
        JNZ Loop 1
        DCR E
        JNZ Loop 2
```

(C) Specify the register contents and the flag status as the following instructions are executed.

	A	B	S	Z	CY
SUB A					
MOV B, A					
ORA B					
SUI 05H					
RAR					
XRA A					

(D) Identify that how many times following loops are execute.

(i)
```
Back: MVI A, FFH
      ORA A
      JC Back
```

(ii)
```
      MVI B, 10H
Back: DCR B
      JNZ Back
```

(iii)
```
      MVI A, 10H
Back: ADI FFH
      CMA
      JP Back
```

END OF PAPER