Student Exam No._____

GANPAT UNIVERSITY

M. Tech. EC Sem-II CBCS REGULAR EXAMINATION April - June 2015

3EC202 DIGITALVLSI DESIGN

TIME: 3 Hrs.] **[TOTAL MARKS: 60**

Instructions: (1) This Question paper has two sections. Attempt each section in separate answer book.
(2) Figures on right indicate marks.
(3) Be precise and to the point in answering the descriptive questions.
(4) Use following data.

SECTION-I

1 (A) Explain constant voltage scaling and its effects on different parameters **(05)**

(B) Consider a resistive-load inverter circuit with V_{DD}=5V, Kn'=20μA/V^2, V_{TO}=0.8V, R_L=200KΩ, and W/L=2. Calculate the V_{OL} and V_{IL} on the VTC. **(05)**

OR

1 (A) Find propagation delay equation for : **(05)**
A. Non buffer case
B. Single buffer case
C. Super buffer case

(B) Explain the five region of operation for CMOS inverter. **(05)**

2 (A) Derive expression for depth of depletion region (Xd) and amount of charge in depletion region (Q) for two terminal MOS. Also find maximum depth of depletion region (Xdm). **(05)**

(B) Draw the following digital circuit using transmission gate **(05)**
1. 4:1 MUX
2. F=AB+A'C'+AB'C

OR

2 (A) Write a short note on : **(05)**
(1) Short Channel Effect
(2) Constant Field Scaling

(B) Justify (W/L)p=2.5(W/L)n for CMOS inverter. **(05)**

3 (A) What is latch-up? Causes of latch-up and how to avoid latch up. **(05)**

(B) Give the difference between CPLD & FPGA. **(05)**

SECTION-II

4 (A) Write a spice code for CMOS inverter for its transient and DC analysis. **(05)**

(B) Explain the types of MOSFET Capacitances. **(05)**

OR

4 (A) Give the comparison of different types of inverter with its VTC. **(05)**

(B) Give the difference between blocking and non-blocking assignment with suitable example. **(05)**

5 (A) Optimize stick diagram layout of a complex CMOS logic gate for following : **(05)**
Half adder

(B) Explain CMOS ring oscillator. **(05)**

OR

5 (A) Write a Verilog code for 8-bit shift-left register with a negative-edge clock, a clock enable, a serial in and a serial out **(05)**

(B) Draw the PLA implementation of following function : **(05)**
F1=XY+X'Z,
F2=Y'+X'Z,
F3=XY+Y'Z

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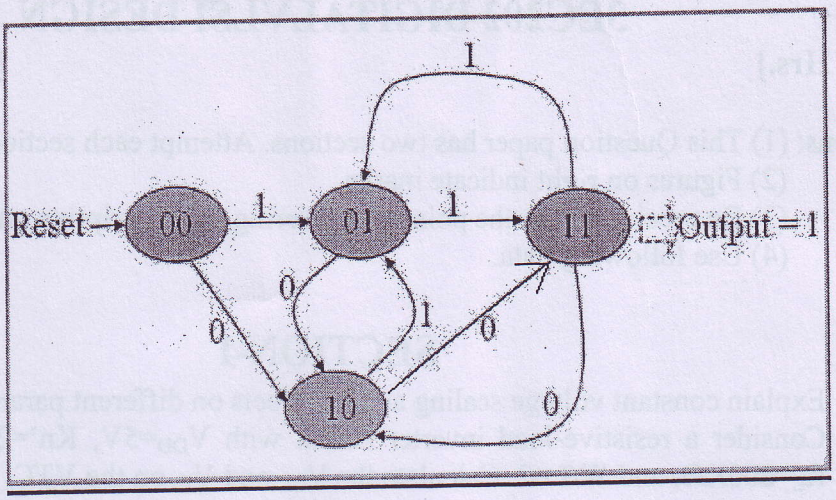
6 (A) What is DOMINO logic? Explain the concept of charge sharing. (05)

(B) Write a verilog code and test bench for following FSM. (05)



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