Student Exam No._____

GANPAT UNIVERSITY

B. Tech. Semester: IV (Biomedical & Instrumentation) Engineering

CBCS Regular Examination April - June 2015

2BM403 Digital Logic Circuits

Total Marks: 70

Time: 3 Hours

Instruction: 1 Write each section in separate answer book.
2 Answer should be brief and to the point.
3 Figure to the right indicates marks.
4 Assume suitable data, if necessary.

Section – I

Que. – 1 12

a) What is the difference between BCD code and Binary code? Convert the decimal number 49 into BCD and binary code.
Also, convert 49 into excess -3 code.

b) Represent the decimal numbers + (positive) 45 and – (negative) 89 as an 8 bit binary number in sign magnitude form. Perform +45 – 89 and -89 + 45 operation using 1's, 2's complement method.

OR 12

Que. – 1

a) Convert the decimal number 123 in following code:
i) Binary Code ii) Octal Code iii) BCD Code
iv) Gray Code v) Excess -3 Code vi) Hexadecimal Code

b) Draw the Half & Full subtractor circuit. Make a truth table for it. Also, draw the timing diagram for half subtractor circuit. 11

Que. – 2

a) Draw the logic diagram of 2 input AND gate, 2 input OR gate and NOT gate using NOR gate only. How many NOT gates are in IC 7404.

b) Simplify the following boolean expression:
[AB' (C + BD) + A'B'] C

c) Prove: i) (A+B) (A+C) = A + BC
ii) A + A'B = A + B

OR 11

Que. – 2

a) Map the following standard SOP expression on a Karnaugh map.
A' B' C D + A' B C' D' + A B C' D + A B C D + A B C' D' + A' B' C' D + A B' C D' + A B' C D
Find the expression and implement it using gates.

b) Define "Multiplexer". Design the logic diagram of 4: 1 multiplexer.

Que. – 3

a) Answer in short:

i) When is the output of AND gate is low? Draw the symbol of 2 input and gate.

ii) How many select lines are required in 8:1 multiplexer?

iii) Determine the values of A, B, C and D that make the product term A`BC`D equal to 1.

iv) How many bits are needed to represent decimal values ranging from 0 to 1622?

v) Determine the weight of 1 in the binary number 1000.

vi) What is the largest decimal number that can be represented in binary with eight bits?

vii) Which gates are known as universal logic gates?

viii) Write the names of non-weighted binary codes.

b) Define "Demultiplexer". Design the logic diagram of 1: 4 demultiplexer.

Section – II 12

Que. – 4

a) What is the normal resting state of NAND gate as a latch? Explain in detail along with logic diagram and timing diagram.

b) What is the function of shift register? Draw and explain 4 bit serial in – serial out shift register.

OR 12

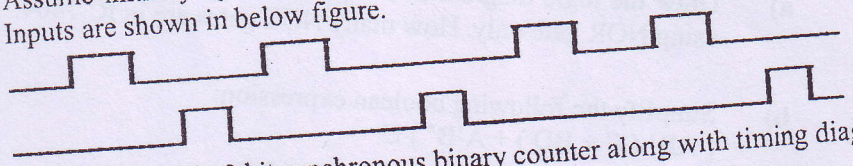
Que. – 4

a) What is the meaning of DCTL and RTL logic? Draw the circuit diagram and explain its working.

b) Explain successive approximation analog to digital converter with circuit diagram. 11

Que. – 5

a) Assume initially Q = 0, Determine Q and Q' waveform for NOR gate latch. Inputs are shown in below figure.



b) Draw and explain 2 bit synchronous binary counter along with timing diagram.

OR 11

Que. – 5

a) Draw and explain J-K flip flop.

b) What is the meaning of "S" and "R" in S-R flip-flow? Draw the logic symbol, logic diagram and explain in detail. 12

Que. – 6

a) What is the meaning of "D" in D type flip-flop? What is its application? Draw the logic symbol, logic diagram and explain in detail.

b) Design Mod – 3 ripple counter.

END OF PAPER