Student Exam No._____

GANPAT UNIVERSITY
B.TECH SEM.4th ELECTRICAL ENGINEERING
REGULAR EXAMINATION APRIL-JUNE 2015
2EE 401:- ANALOG AND DIGITAL ELECTRONICS

TIME:-3 HOURS **TOTAL MARKS-70**

INSTRUCTION:-
1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

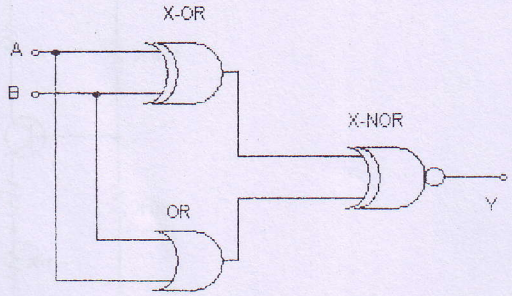
Section-I

Que-1

(a) What is half subtractor circuit? Explain half subtractor circuit by using truth table and logic circuit. **(04)**

(b) Show that $A \odot B = \overline{A \oplus B}$. Also, construct the corresponding logic diagrams. **(04)**

(c) Redraw the circuit given in below figure after simplification. **(04)**



OR

Que-1

(a) Explain Following terms: Minterm, Maxterm, SOP, POS. **(04)**

(b) Explain 2 to 1 decoder with bock diagram, truth table and logic circuit. **(04)**

(c) Draw the logic symbols, construct the truth tables, and with the help of circuit diagrams of AND gate, OR gate, NOT gate. **(04)**

Que-2

(a) Reduce the expression $f = \bar{A}\bar{B} + \bar{A}B + AB$ using K-map. **(03)**

(b) State and explain De-Morgan's theorem with logic gates. **(04)**

(c) Explain 2 to 1 multiplexer with bock diagram, truth table and logic circuit. **(04)**

OR

Que-2

(a) Explain T flip flop with necessary diagram and truth table. **(04)**

(b) Add -31.5 to -93.125 using the 12-bit 2's complement arithmetic **(03)**

(c) Discuss the application of the counter. **(04)**

Que-3 **Attempt any six.** **(12)**

(a) Convert $(11011)_{Gray}$ to binary code.

(b) Convert $(943)_{10}$ to BCD code.

(c) Multiply $(1001)_2$ by $(1101)_2$

(d) Convert $(675.625)_{10}$ to Hexadecimal.

(e) Convert $(11011.101)_2$ to decimal

(f) Comparison between combinational and sequential circuit.

(g) Plot the expression $f = (A + B)(\bar{A} + B)(\bar{A} + \bar{B})$ on the K-map.

(i) What do you mean by self-complement codes? Give examples.

Section-II

Que-4

(a) What are the basic conditions for transistor biasing? Explain base resistor circuit and give our conclusion for this method. (06)

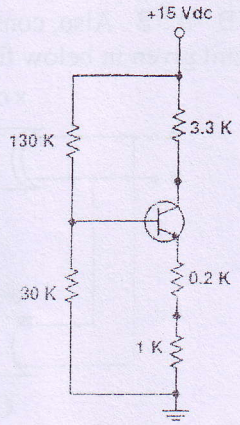
(b) Discuss the working principle of Junction Field Effect Transistor. Explain its characteristics with necessary diagrams (06)

OR

Que-4

(a) Illustrate the operation of common base connection of transistor. Derive the expressions for collector current. (06)

(b) Draw a DC load line and determine the operating point. Assume transistor of silicon. (06)



Que-5

(a) Draw and explain the Differentiator circuit and show that it's output will be the integral of input signal. (06)

(b) Discuss the square wave generator circuit using op-amp. (05)

OR

Que-5

(a) Brief about the operation of inverting amplifier with feedback. Establish the relation between open loop gain (A), closed loop gain (AF) and gain of feedback circuit (B) for the same. (06)

(b) Design a practical integrator circuit to properly process input signal of 1 kHz to 10 kHz. If a square wave signal of 5V peak at 10 kHz frequency is applied as a input to differentiator, Draw its output waveform. (05)

Que-6 **Attempt any three.** (12)

(a) Define following :
i) CMRR, ii) Output Voltage Swing, iii) SVRR, iv) Pinch off voltage

(b) An Op-amp having the following parameters is connected as inverting amplifier with R1 = 3 kΩ and Rf = 12kΩ, A = 250000 , Ri = 2.2MΩ, Ro = 100 Ω , fo = 5 Hz, Vs = ± 15 V and output voltage swing = ± 13 V. Compute the values of AF, RiF, RoF, and fF.

(c) Discuss the operation of IC 555 as mono-stable multivibrator.

(d) Give the difference between BJT and JFET.

----------END OF PAPER----------