M.Tech Evening Date: 27/05/2015

Exam No. _____

GANPAT UNIVERSITY

M. Tech. Semester-II (CE) Regular Examination (April-June 2015)

3CE202 : Advanced Computer Architecture

Time: 3 Hours] **[Total Marks: 60**

Instruction: 1 All questions are compulsory.
2 Answer both sections in separate answer sheets.

SECTION - I

Q-1. **(A)** Calculate delay in number of clock cycle, due to data dependency for the following instructions. **[5]**

Instr. 1. DIV R1,R2,R3 / C(R1) <- C(R2) / C(R3)
Instr. 2. SUB R3,R4,R5 / C(R3) <- C(R4) - C(R5)
Instr. 3. DEC R2 / C(R2) <- C(R2) - 1
Instr. 4. ADD R5,R6,R7 / C(R5) <- C(R6) + C(R7)

Apply pipeline lock and again calculate the delay with for the same problem.

(B) Define internal forwarding technique with its types and apply it for the following operations in a sequence. Draw data flow graph and make compound function after applying this method. **[5]**

1. $R_1 \leftarrow (M_1)$ (fetch)
2. $R_1 \leftarrow (R_1) / (M_2)$ (divide)
3. $R_1 \leftarrow (R_1) + (M_3)$ (add)
4. $M_4 \leftarrow (R_1)$ (store)

OR

Q-1. **(A)** Explain different classification schemes of pipeline processors with figure. **[5]**

(B) Define non linear pipelines? Explain that such pipelines are configured for multiple outputs and draw reservation table for given example. **[5]**

Q-2. **(A)** Explain two configurations of SIMD array processor with figure and mention two differences between them. **[5]**

(B) Explain direct mapping technique for mapping of main memory to cache memory. **[5]**

OR

Q-2. **(A)** Explain fully associative mapping for cache memory. **[5]**

(B) Describe super scalar processor with state time diagram and its features. Derive equation to find speedup of the superscalar machine over the base machine. **[5]**

Q-3. **(A)** "Synchronization in Pipeline processing is essential". State True or False & justify your answer with example pipeline diagram. **[4]**

(B) Evaluate data dependences among the statements of the following program and draw dependency graph: **[6]**

S1: LOAD R_A, M[10] /$R_A \leftarrow$ M[10]
S2: LOAD R_B, M[45] /$R_B \leftarrow$ M[45]
S3: ADD R_A, R_B /$R_A \leftarrow R_A + R_B$
S4: DIV R_A, 7 /$R_A \leftarrow R_A / 7$
S5: STORE M[20], R_A /M[20] $\leftarrow R_A$

SECTION – II

Q-4. (A) Explain overlapping register windows concept in RISC with figure. [5]

(B) For SIMD architecture, draw diagram and describe significance of generalized multiprocessor system containing IPMN, PION, and IPCN networks. [5]

OR

Q-4. (A) Explain attributes of RISC architecture and compare it with CISC. [5]

(B) Explain use of compensation code in upward and downward code motion in trace scheduling with diagram for VLIW. [5]

Q-5. (A) Define: Bisection width and what are the factors affecting the performance of an interconnection network and why? [5]

(B) Explain concept of VLIW and what are the possible problems in VLIW? [5]

OR

Q-5. (A) Explain I-Structure as a synchronization mechanism in dataflow computer architecture with diagram. [5]

(B) Draw its architectural diagram of ULTRA SPARC IV plus and list out its features. [5]

Q-6. (A) Take one example to explain benefits of masking and data routing mechanism in Illiac IV. [5]

(B) Calculate, miss penalty for (1) 2 words wide and (2) 4 words wide Interleaved memory organizations, for the following: [5]

1 clock cycle to send the address
15 clock cycles for each DRAM access initiated
1 clock cycle to send a word of data
4 word cache block and 1 word wide DRAM bank.

--- END OF PAPER ---