Seat No._____

GANPAT UNIVERSITY

M. Tech. Semester: II Computer Engineering

Regular Examination July-2013

3CE202:Advanced Computer Architecture

Time: 3 Hours] **[Total Marks: 70**

Instruction: 1 All questions are compulsory.
2 Answer both sections in separate answer sheets.

SECTION - I

Q-1. (A) Consider the following pipeline reservation table. **7**

	0	1	2	3	4	5	6	7	8
S1	X								X
S2		X	X					X	
S3				X					
S4					X	X			
S5							X	X	

(1) What are the forbidden latencies?
(2) Draw the state transition diagram.
(3) List all the simple cycles and greedy cycles.
(4) Determine the minimum average latency.

(B) The main memory is assumed to have 4K pages, each page having 16 words while the cache has 128 pages. Then calculate no. of bits in a tag field and address of CAM word for (i) 4 pages per set (ii) 64 pages per set **4**

Q-2. (A) Analyze the data dependences of the statements of the following program : **6**

S1: LOAD R1, M[100] /R1 ← M[100]
S2: LOAD R2, M[104] /R2 ← M[104]
S3: MULT R1, R2 /R1 ← R1 * R2
S4: INC R1 /RA1← R1 + 1
S5: STORE M[110], R1 /M[110] ←R1

(1) Draw a dependency graph to show all the dependences:
(2) Is there any resource dependences if only one copy of each functional unit is available in the CPU?

(B) Explain direct mapping technique for mapping of main memory to cache memory. **6**

OR

Q-2. (A) Explain associative mapping technique with CAM word organization. **6**

(B) Explain Branch prediction buffer method to reduce delay due to branch instructions. **6**

Q-3. (A) Find out delay due to data dependency for the following instructions. **6**

Instr. 1. LOAD R2,R3, Y / C(R2) <- C(Y+C(R3))
Instr. 2. ADD R1,R2,R3 / C(R3) <- C(R1)+C(R2)
Instr. 3. MUL R4,R3,R1 / C(R1) <- C(R4)*C(R3)
Instr. 4. SUB R7,R8,R9 / C(R9) <- C(R7)-C(R8)

Also calculate the delay with pipeline lock for the same problem.

(B) Explain data buffering and busing structures as a principle of designing pipeline processors. **6**

OR

Q-3. (A) An examination paper has 4 questions and total number of answer books are 1000. each question takes 5 minutes to correct. If 4 teachers are employed for correction in pipeline mode. Then calculate the speedup and efficiency. **6**

(B) Apply internal forwarding technique for the following operations in a sequence. Draw data flow graph and make compound function after applying this method. 6

1. $R_0 \leftarrow (M_1)$ (fetch)
2. $R_0 \leftarrow (R_0) + (M_2)$ (add)
3. $R_0 \leftarrow (R_0) * (M_3)$ (multiply)
4. $M_4 \leftarrow (R_0)$ (store)

SECTION - I

Q-4. (A) What is the basis of VLIW? Why this machine is incompatible with other machines? What are the problem in compaction? 7

(B) Explain Node Degree and Bisection Width with example 4

Q-5. (A) Why RISC is considered as better performing machine ? what are important features of ULTRA SPARC IV plus? Explain with architectural diagram. 6

(B) What is the purpose of Overlapping Register Windows in RISC ? Explain Register windows with figure. 6

OR

Q-5. (A) Compare Super scalar processor with super pipeline processor using state time diagram and its features. 6

(B) How many steps are required to route data from PE*i* to any other PE*j* in an Illiac network of N=16 PEs? Justify your answer. 6

Q-6. (A) Show that a Data flow computer is highly parallel with example. 6

(B) What are different Vector Instructions used in a typical vector computer? How S-access memory organization is useful in such computers. 6

OR

Q-6. (A) Explain masking and data routing mechanism of Illiac IV with the help of PE (Processing Elements) and its all registers. 6

(B) Mention Amdahl's law and explain with an example. 6

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